

Compal Confidential

G400S/G500S DIS M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

nVIDIA N14X

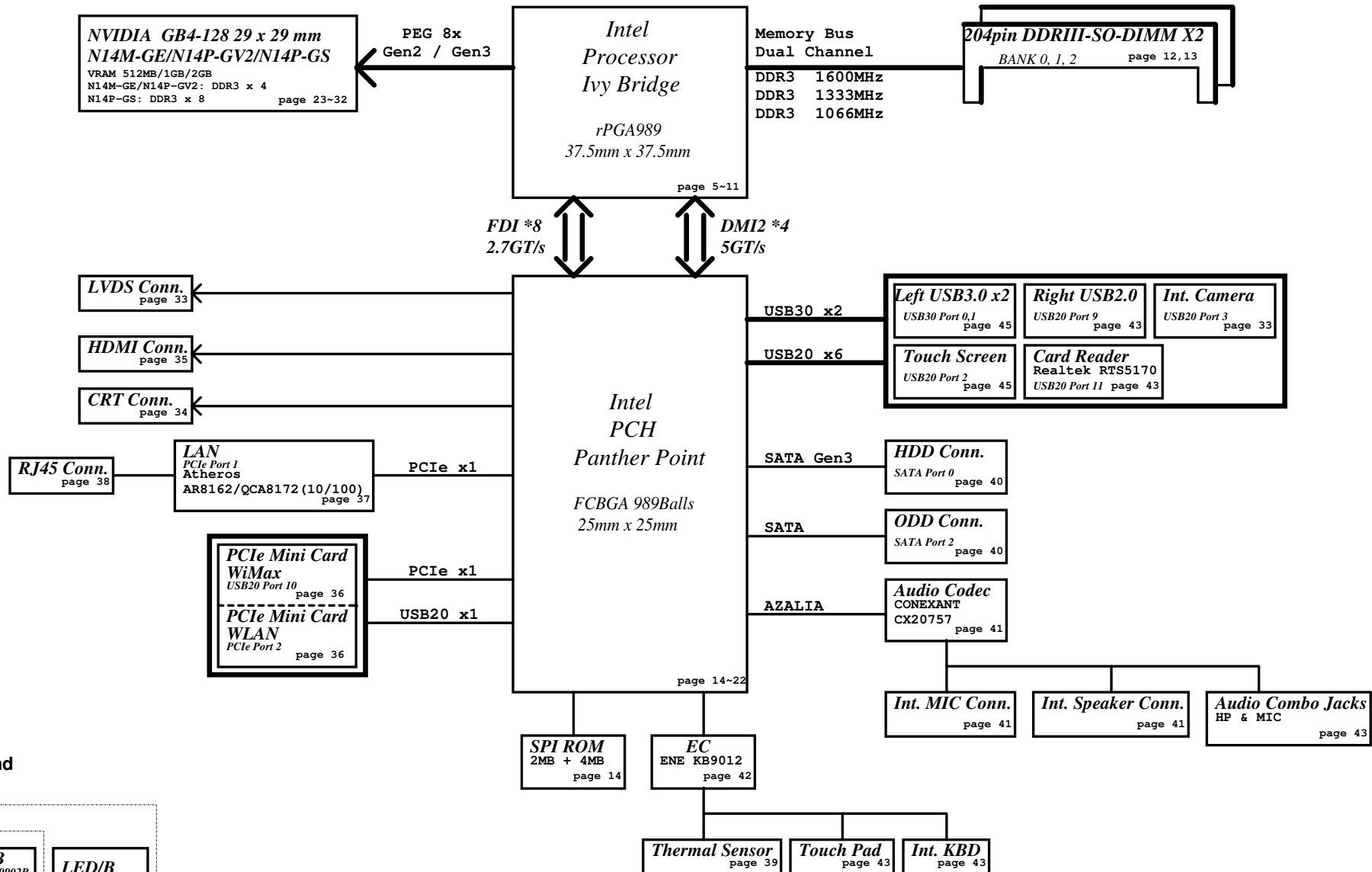
LA-9901P

2013-03-20

REV:1.0

| | | | | |
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| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 | Title |
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| | | | | Rev |
| | | | | 1.0 |
| | | | | Wednesday, March 20, 2013 |
| | | | | Sheet 1 of 63 |

Chief River



| | | | | | |
|---|--------------------|-----------------|------------|--------------------------|-------------------------------|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 | Title | MB Block Diagram |
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| | | | | Date | Wednesday, March 20, 2013 |
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| | | | | Rev | 1.0 |

Voltage Rails

| power plane | State | +B | +5VALW +3VALW | +1.5V | +5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC GFXCORE_AXG +1.8VS +0.75VS +1.05VS |
|--------------------------------|-------|----|------------------|-------|--|
| S0 | O | O | O | O | O |
| S3 | O | O | O | O | X |
| S5 S4/AC | O | O | O | X | X |
| S5 S4/ Battery only | O | X | X | X | X |
| S5 S4/AC & Battery don't exist | X | X | X | X | X |

EC SM Bus1 address

| Device | Address |
|---------------|-------------|
| Smart Battery | 0001 011X b |

EC SM Bus2 address

| Device | Address |
|----------------|------------|
| Thermal Sensor | 1001 100xb |

PCH SM Bus address

| Device | Address |
|-----------|------------|
| DDR DIMM0 | 1010 000Xb |
| DDR DIMM2 | 1010 010Xb |

NV-GPU SM Bus address

| Device | Address |
|-------------------------|-------------------|
| Internal thermal sensor | 1001 111Xb (0x9E) |

BOARD ID Table

| Board ID | PCB Revision |
|----------|--------------|
| 0 | 1.0 |
| 1 | 0.3 |
| 2 | 0.2 |
| 3 | 0.1 |
| 4 | |
| 5 | |
| 6 | |
| 7 | |

| STATE | SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V | +VS | Clock |
|-----------------------|--------|---------|---------|---------|---------|-------|-----|-----|-------|
| Full ON | | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S1 (Power On Suspend) | | LOW | HIGH | HIGH | HIGH | ON | ON | ON | LOW |
| S3 (Suspend to RAM) | | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | | LOW | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF |

Board ID table for AD channel

| | | | | | | |
|----------|-------------|-------------|-------------|-------------|-------------|-----|
| Vcc | 3.3V | | | | | |
| Ra | 100K +/- 1% | | | | | |
| Board ID | Rb | VAD_BID min | VAD_BID typ | VAD_BID max | EC AD | |
| 0 | 0 | 0 V | 0 V | 0.300 V | 0x00 – 0x0B | MP |
| 1 | 12K +/- 1% | 0.347 V | 0.354 V | 0.360 V | 0x0C – 0x1C | PVT |
| 2 | 15K +/- 1% | 0.423 V | 0.430 V | 0.438 V | 0x1D – 0x26 | DVT |
| 3 | 20K +/- 1% | 0.541 V | 0.550 V | 0.559 V | 0x27 – 0x30 | EVT |

USB Port Table

| | USB 2.0 | Port | 3 External USB Port |
|--------------|---------|------|-----------------------------|
| EHCI1 USB3.0 | UHCI0 | 0 | USB Port (Left Side) USB3.0 |
| | | 1 | USB Port (Left Side) USB3.0 |
| | UHCI1 | 2 | Touch Screen |
| | | 3 | USB Camera |
| | UHCI2 | 4 | |
| | | 5 | |
| EHCI2 | UHCI3 | 6 | |
| | | 7 | |
| | UHCI4 | 8 | |
| | | 9 | USB/B (Right Side USB2.0) |
| | UHCI5 | 10 | Mini Card(WLAN) |
| | | 11 | Card Reader |
| | UHCI6 | 12 | |
| | | 13 | |

BOM Structure Table

| BTO Item | BOM Structure |
|-----------------------|---------------|
| 45 LEVEL | 45@ |
| Connector | ME@ |
| For VILG2 (14") | 14@ |
| For VILG1 (15") | 15@ |
| GPU:N14M-GE | N14@ |
| HDMI | HDMI@ |
| Camera | CMOS@ |
| LAN LDO Mode | LDO@ |
| LAN Switch mode | SWR@ |
| 10/100 LAN (AR8162L) | 8162@ |
| 10/100 LAN (QCA8172) | 8172@ |
| N14M-GE SKU | GE@ |
| N14P-GS SKU | GS@ |
| N14P-GV2 SKU | GV2@ |
| N14P-GV2&N14P-GS SKU | GVGS@ |
| Green clock (DIS sku) | GCLK304@ |
| Green clock (UMA sku) | GCLK244@ |
| Green clk support | GCLK@ |
| No Green clk support | NOGCLK@ |
| Nvidia GC6 state | GC6@ |
| Touch Screen SKU | TS@ |
| Optimus SKU | OPT@ |
| UMA SKU | UMA@ |
| PCH (NM70 sku) | NM70@ |
| PCH (HM70 sku) | HM70@ |
| PCH (HM76 sku) | HM76@ |
| VRAM (1000MHz) | 1000M@ |
| VRAM (900MHz) | 900M@ |
| Unpop | @ |

SMBUS Control Table

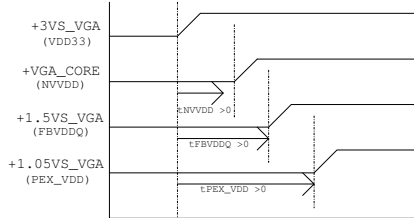
| | SOURCE | VGA | BATT | KB9012 | SODIMM | WLAN | Thermal Sensor | PCH |
|------------|--------|----------|--------|--------|--------|------|----------------|------|
| SMB_EC_CK1 | KB9012 | X | V | X | X | X | X | X |
| SMB_EC_DA1 | +3VALW | | +3VALW | | | | | |
| SMB_EC_CK2 | KB9012 | V | X | X | X | X | X | V |
| SMB_EC_DA2 | +3VALW | +3VS_VGA | | | | | | +3VS |
| SMBCLK | PCH | X | X | X | V | V | X | X |
| SMBDATA | +3VALW | | | | +3VS | +3VS | | |
| SML0CLK | PCH | X | X | X | X | X | X | X |
| SML0DATA | +3VALW | | | | | | | |
| SML1CLK | PCH | V | X | V | X | X | V | X |
| SML1DATA | +3VALW | +3VS_VGA | | +3VS | | | +3VS | |

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N14x GPIO Pin Definition Table

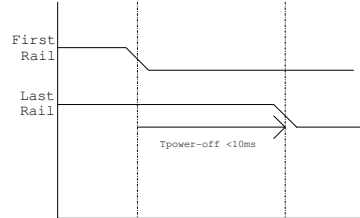
| Pin Name | Normal Function | I/O | Functional Description | Default PU/PD |
|-----------|---------------------|-----|--|---------------------------------|
| GPIO0 | FB_CLAMP_MON | I | FB Clamp monitor | |
| GPIO1 | MEM_VDD_CTL | O | Memory VDD VID | MEM VID Strap to boot FBVDD/Q |
| GPIO2-4 | Non-support for LCD | O | Panel | 100k PD |
| GPIO5 | Reserve | | | |
| GPIO6 | FB_CLAMP_TGL_REQ# | O | Active low FB Clamp toggle request | |
| GPIO7 | 3DVision | O | 3D Vision L/R signal | 100k PD |
| GPIO8 | OVERT | IO | Active Low Thermal Catastrophic Over Temperature | 100k PU |
| GPIO9 | ALERT | IO | Active Low Thermal Alert | 100k PU |
| GPIO10 | MEM_VREF_CTL | O | Memory VREF Control | 100k PD |
| GPIO11 | PWM_VID | O | GPU Core VDD PWM control supply overdraw input | |
| GPIO12 | PWR_LEVEL | I | AC power detect or control signal | 100k PU |
| GPIO13 | PSI | O | Phase Shedding | PSI:100k PU to enable two phase |
| GPIO14-19 | Non-support for HDA | I | Hot Plug | |
| GPIO20-21 | Reserve | | | |

GPU Power On



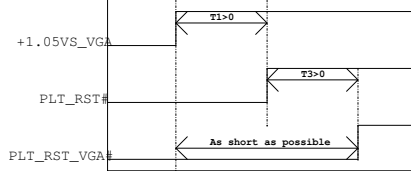
1. all power rail ramp up time should be larger than 40us
2. The total time for all rails to ramp should be within 6ms.
3. A power rail has to ramp up 90% before the next power rail in sequence can start ramping up.
4. No signal should be applied to the GPU before the power rail are fully ramped.

GPU Power Down

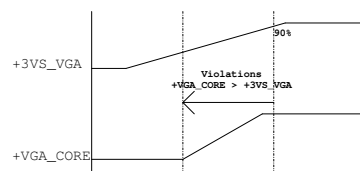


1. All GPU power rails should be turned off within 10ms

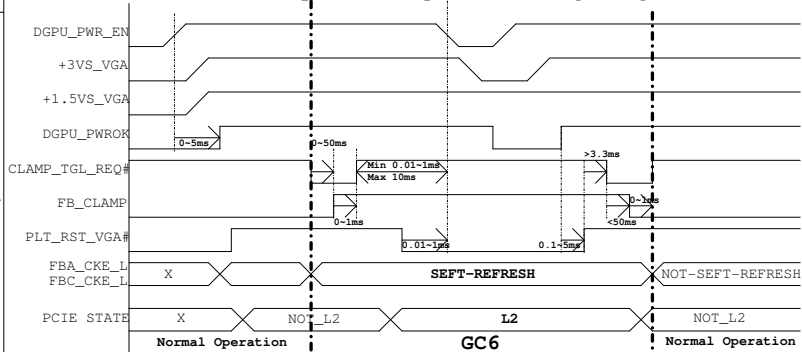
GPU Reset Sequence



Power sequencing violations



GC6 Entry/Exit Sequence Timing Diagram



For N14P-GV2 strap table X76

| GPU | Frenq. | Memory Size | Memory Config | strap0 | strap1 | strap2 | strap3 | strap4 | ROM_SI | ROM_SO | ROM_SCLK |
|----------|---------|------------------|--------------------------------|--------|--------|--------|--------|--------|--------|--------|----------|
| N14P-GV2 | 1 GHz | 128M*16*4 1GB | Samsung K4W2G1646E-BC1A | R | R | R | R | R | R | R | R |
| N14P-GV2 | 1 GHz | 128M*16*4 1GB | Micron MT41J128M16JT-093G-K | PU 45K | PD 45K | PD 15K | PD 5K | PD 45K | PD 45K | PU 5K | PU 5K |
| N14P-GV2 | 1 GHz | 128M*16*4 1GB | Hynix H5TC2G63FFR-11C | R | R | R | R | R | R | R | R |
| N14P-GV2 | 900 MHz | 256M*16*4 2GB | Samsung K4W4G1646B-HC11 | PU 45K | PD 45K | PD 15K | PD 5K | PD 45K | PD 20K | PU 5K | PU 5K |
| N14P-GV2 | 900 MHz | 256M*16*4 2GB | Micron MT41K256M16HA-107G-E | PU 45K | PD 45K | PD 15K | PD 5K | PD 45K | PD 10K | PU 5K | PU 5K |

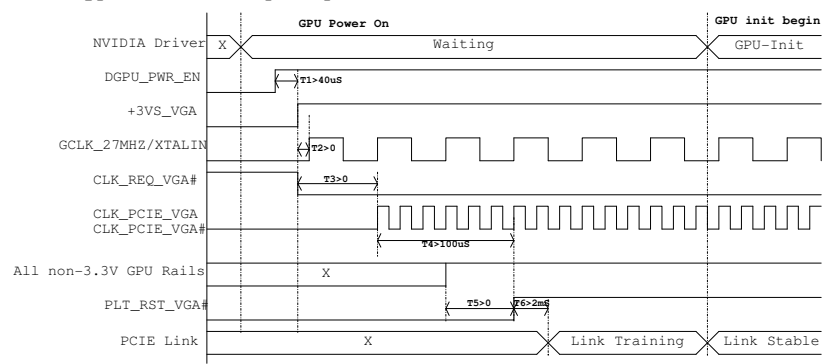
For N14P-GS strap table X76

| GPU | Frenq. | Memory Size | Memory Config | strap0 | strap1 | strap2 | strap3 | strap4 | ROM_SI | ROM_SO | ROM_SCLK |
|---------|---------|------------------|--------------------------------|--------|--------|--------|--------|--------|--------|--------|----------|
| N14P-GS | 1 GHz | 128M*16*8 2GB | Samsung K4W2G1646E-BC1A | R | R | R | R | R | R | R | R |
| N14P-GS | 1 GHz | 128M*16*8 2GB | Micron MT41J128M16JT-093G-K | PU 45K | PD 5K | PD 20K | PD 5K | PD 45K | PD 45K | PU 5K | PD 15K |
| N14P-GS | 1 GHz | 128M*16*8 2GB | Hynix H5TC2G63FFR-11C | R | R | R | R | R | R | R | R |
| N14P-GS | 900 MHz | 256M*16*8 2GB | Samsung K4W4G1646B-HC11 | PU 45K | PD 5K | PD 20K | PD 5K | PD 45K | PD 20K | PU 5K | PD 15K |
| N14P-GS | 900 MHz | 256M*16*8 4GB | Micron MT41K256M16HA-107G-E | PU 45K | PD 5K | PD 20K | PD 5K | PD 45K | PD 10K | PU 5K | PD 15K |

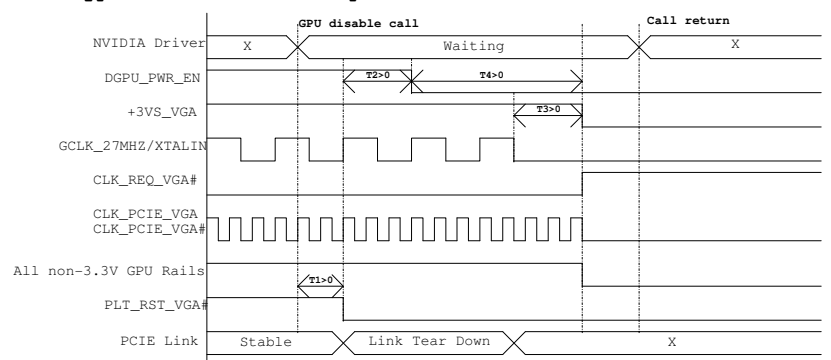
For N14M-GE strap table X76

| GPU | Frenq. | Memory Size | Memory Config | strap0 | strap1 | strap2 | strap3 | strap4 | ROM_SI | ROM_SO | ROM_SCLK |
|---------|---------|------------------|--------------------------------|--------|--------|--------|--------|--------|--------|--------|----------|
| N14M-GE | 1 GHz | 128M*16*4 1GB | Samsung K4W2G1646E-BC1A | R | PU 10K | R | R | R | R | R | R |
| N14M-GE | 1 GHz | 128M*16*4 1GB | Micron MT41J128M16JT-093G-K | PU 10K | PD 10K | PD 10K | PD 10K | PD 10K | PD 10K | PD 10K | PD 10K |
| N14M-GE | 1 GHz | 128M*16*4 1GB | Hynix H5TC2G63FFR-11C | R | R | R | R | R | R | R | R |
| N14M-GE | 900 MHz | 256M*16*4 2GB | Samsung K4W4G1646B-HC11 | PU 10K | PD 10K | PD 10K | PD 10K | PD 10K | PD 10K | PD 10K | PD 10K |
| N14M-GE | 900 MHz | 256M*16*4 2GB | Micron MT41K256M16HA-107G-E | PU 10K | PD 10K | PD 10K | PD 10K | PD 10K | PD 10K | PD 10K | PD 10K |

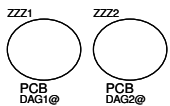
Optimus Typical Power-Up Sequence



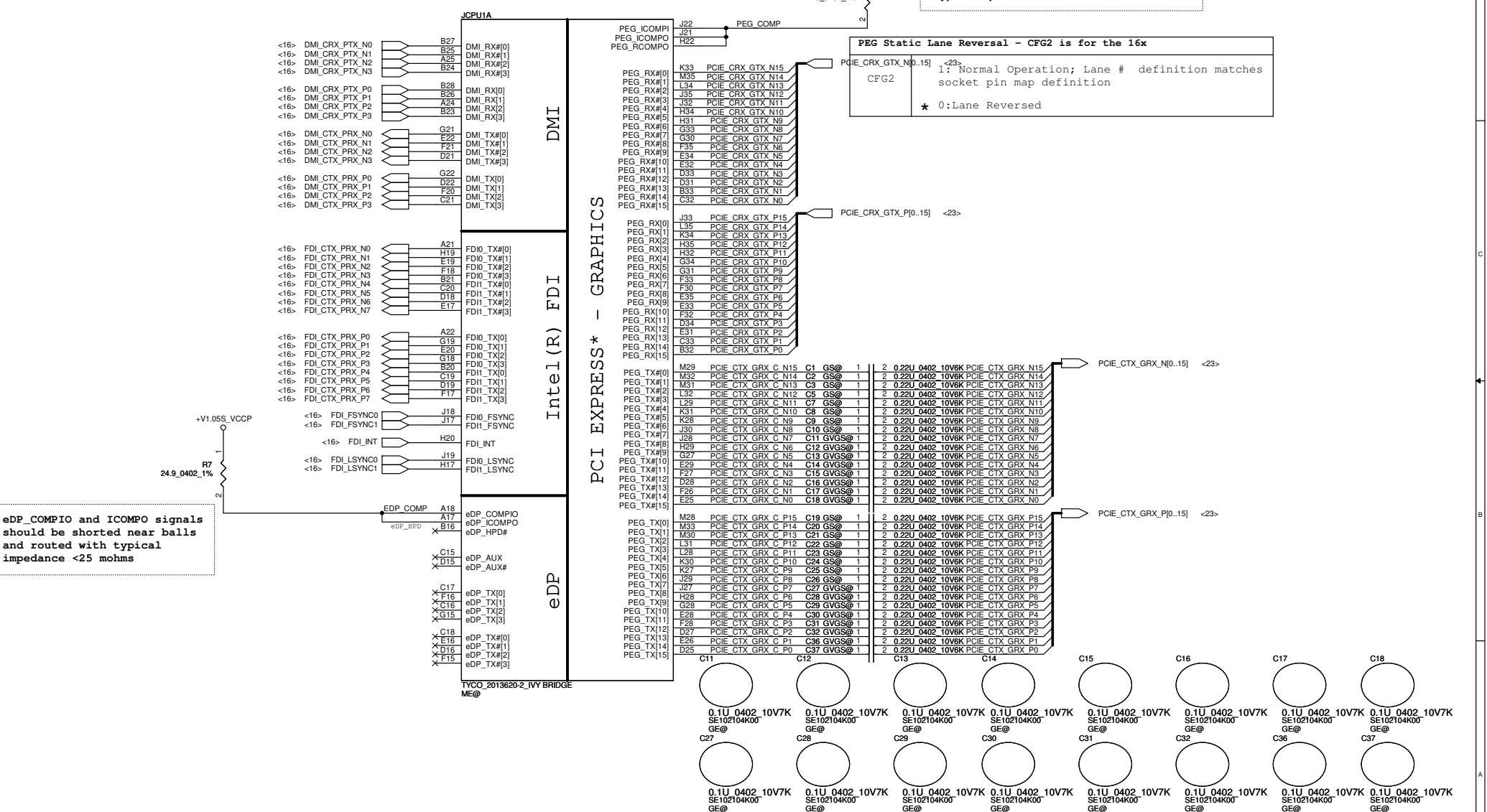
Optimus Typical Power-Down Sequence



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| | | | | VILG1/G2 MB LA-9901P Schematic | 0.3 | |
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PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG Static Lane Reversal - CFG2 is for the 16x
1: Normal Operation; Lane # definition matches socket pin map definition
* 0: Lane Reversed

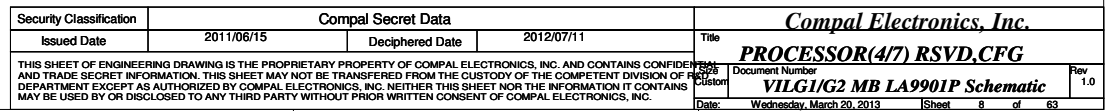
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| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 | PROCESSOR(1/7) DMI,FDI,PEG | |
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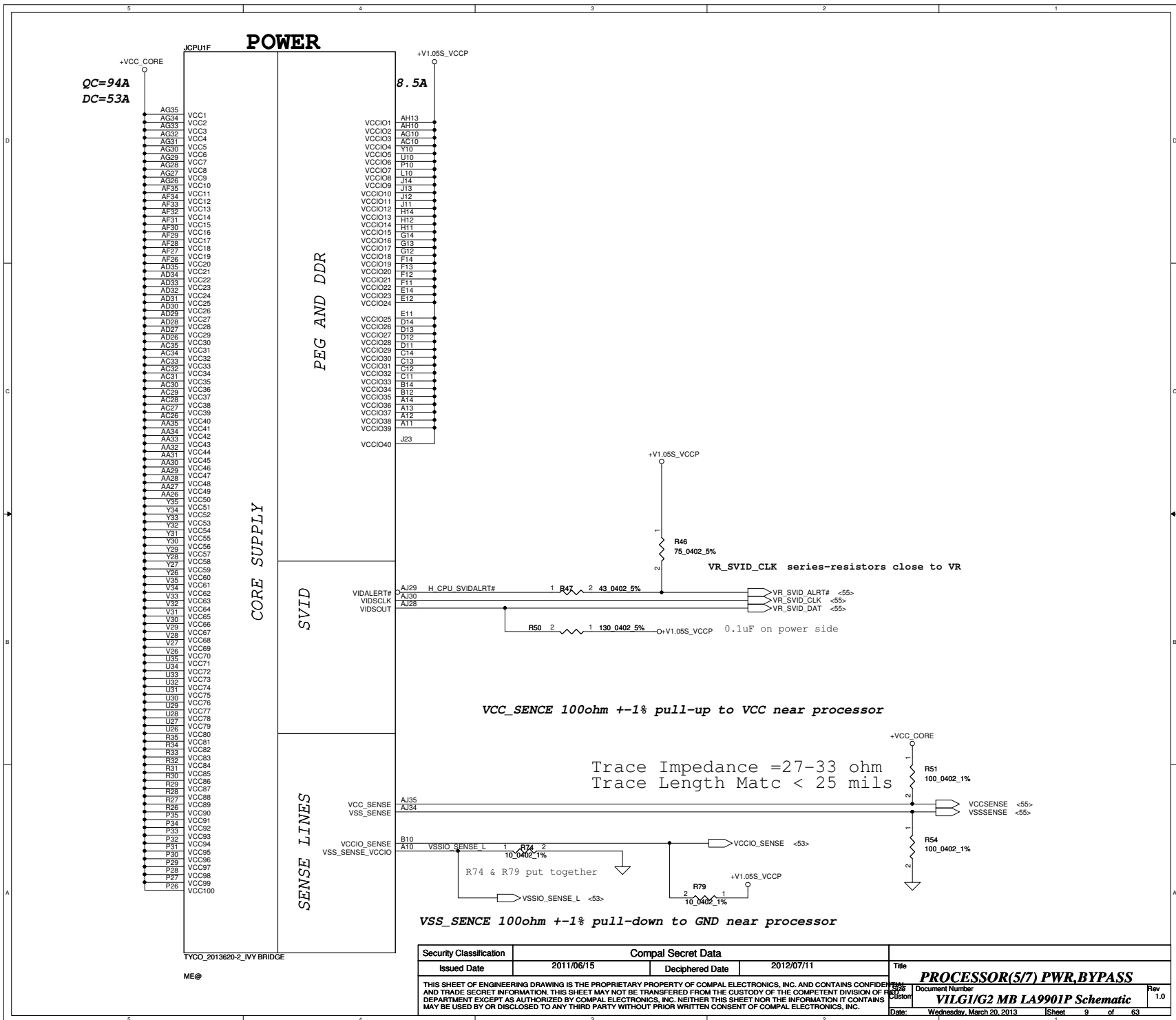
| | |
|------|--|
| CFG2 | 1: Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed |
|------|--|

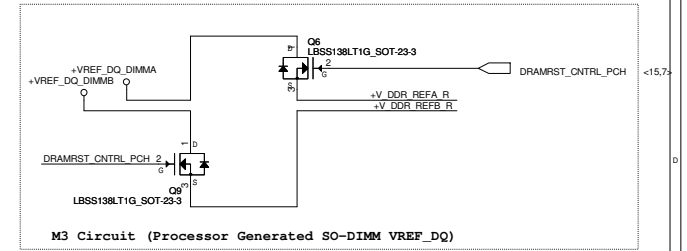
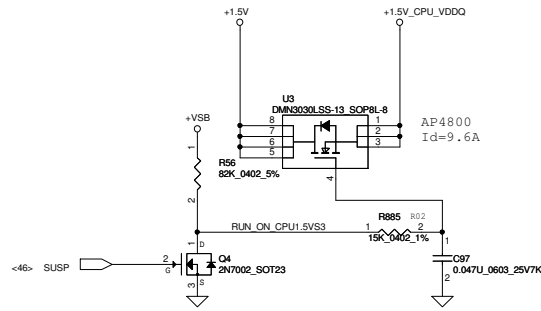
| | |
|------|---|
| CFG4 | <p>* 1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p> |
|------|---|

| | |
|----------|--|
| | 11: (Default) x16 - Device 1 functions 1 and 2 disabled |
| CFG[6:5] | *10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled |
| | 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) |
| | 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled |

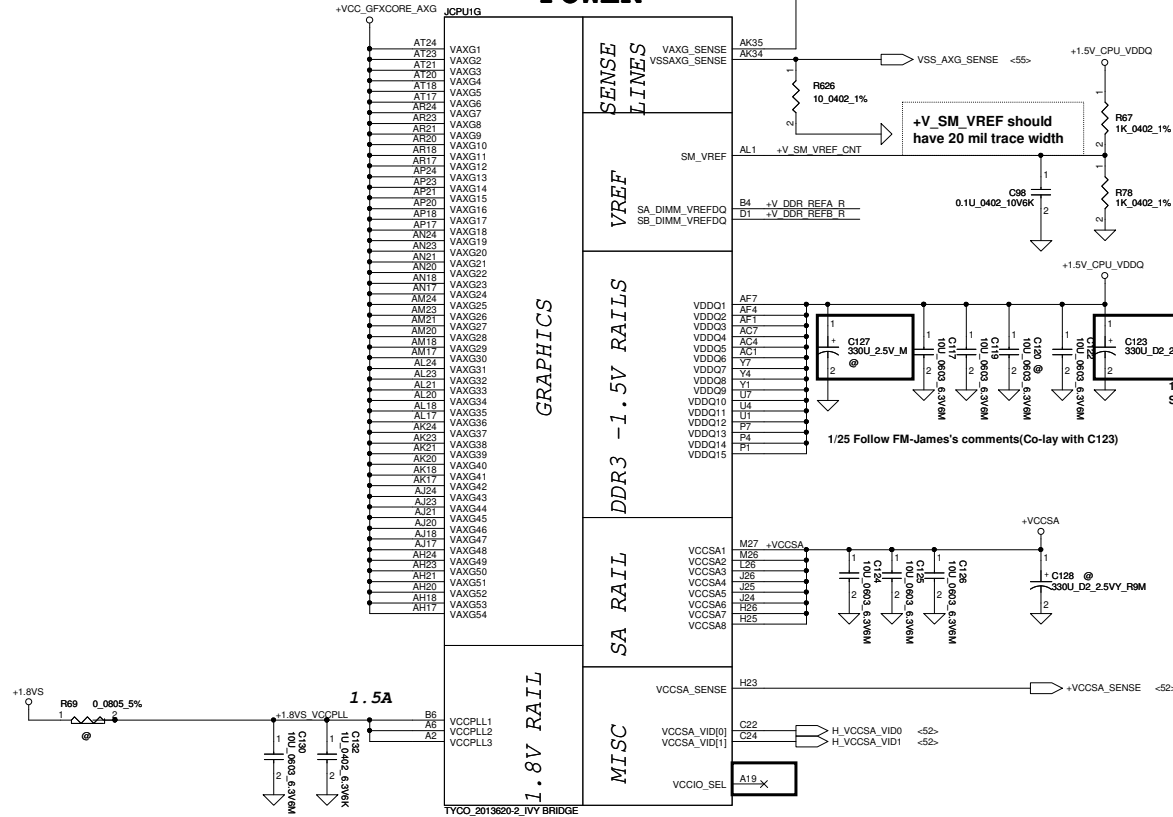
| | |
|------|---|
| CFG7 | 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training |
|------|---|







POWER

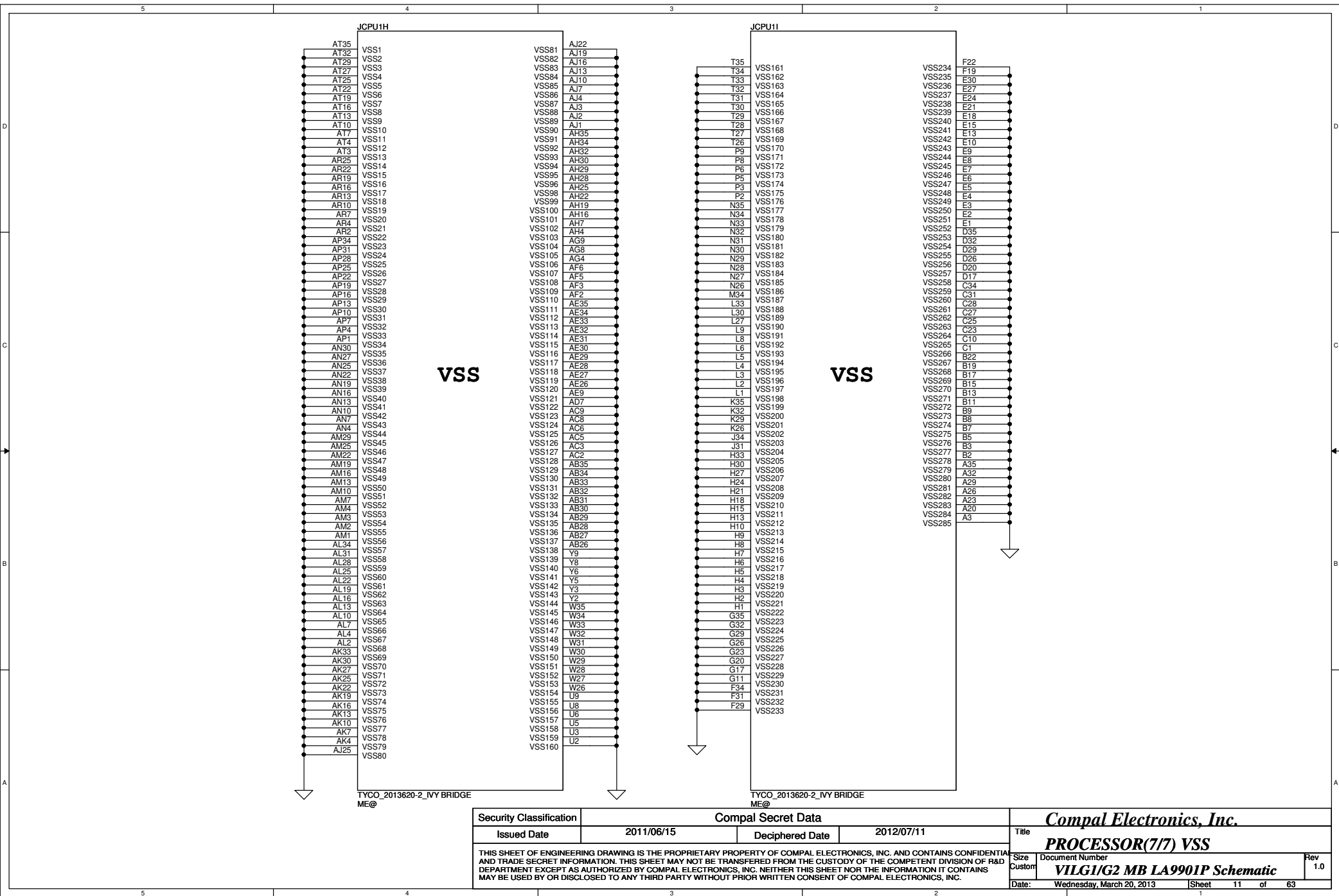


1/16 Change symbol & value from SF000002Z00 to SGA20331E10

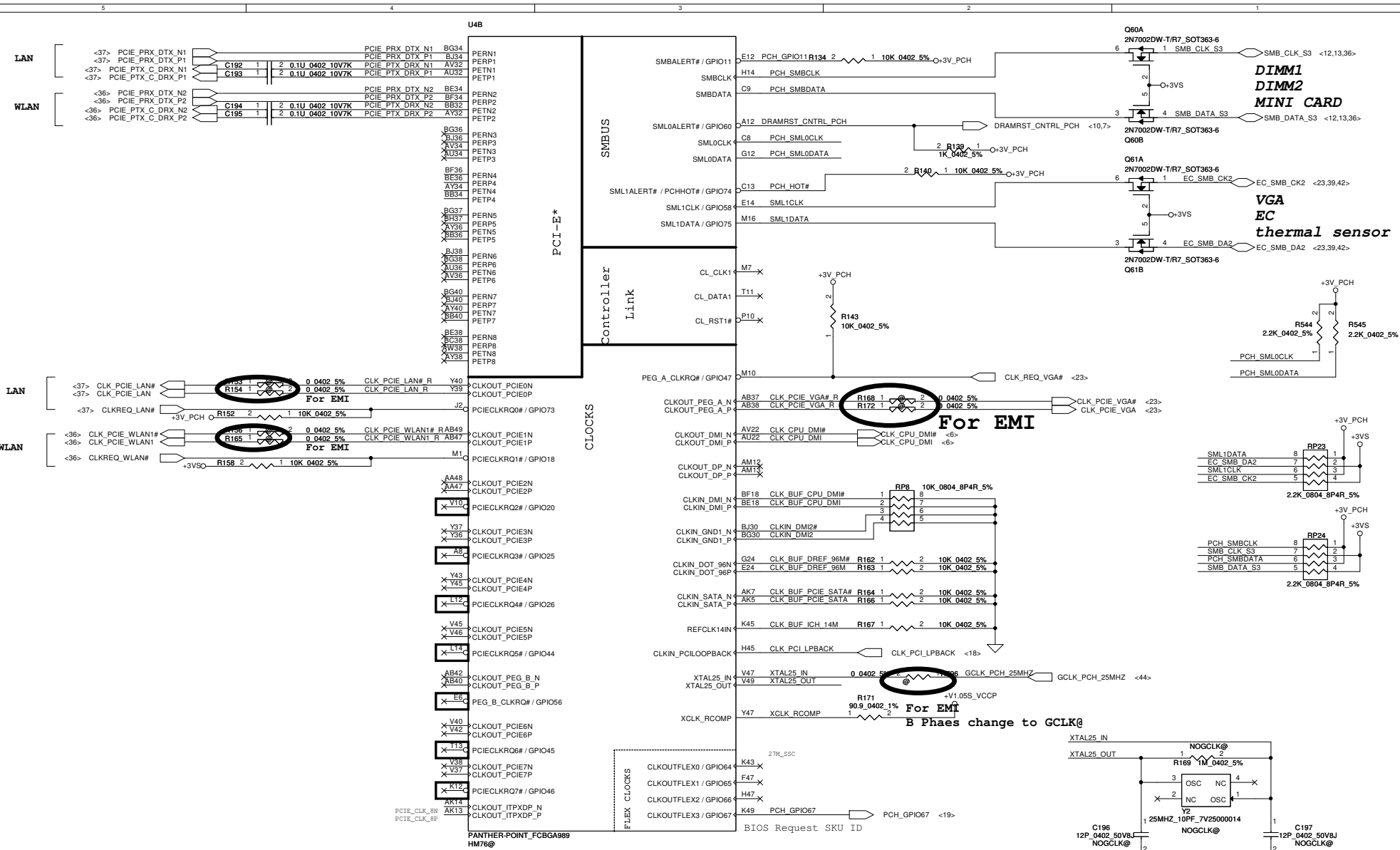
1/25 Follow FM-James's comments(Co-lay with C123)

IVY Bridge drives VCCIO_SEL low
VCCP_PWRCTRL:0
Sandy Bridge is NC for A19
VCCP_PWRCTRL:1

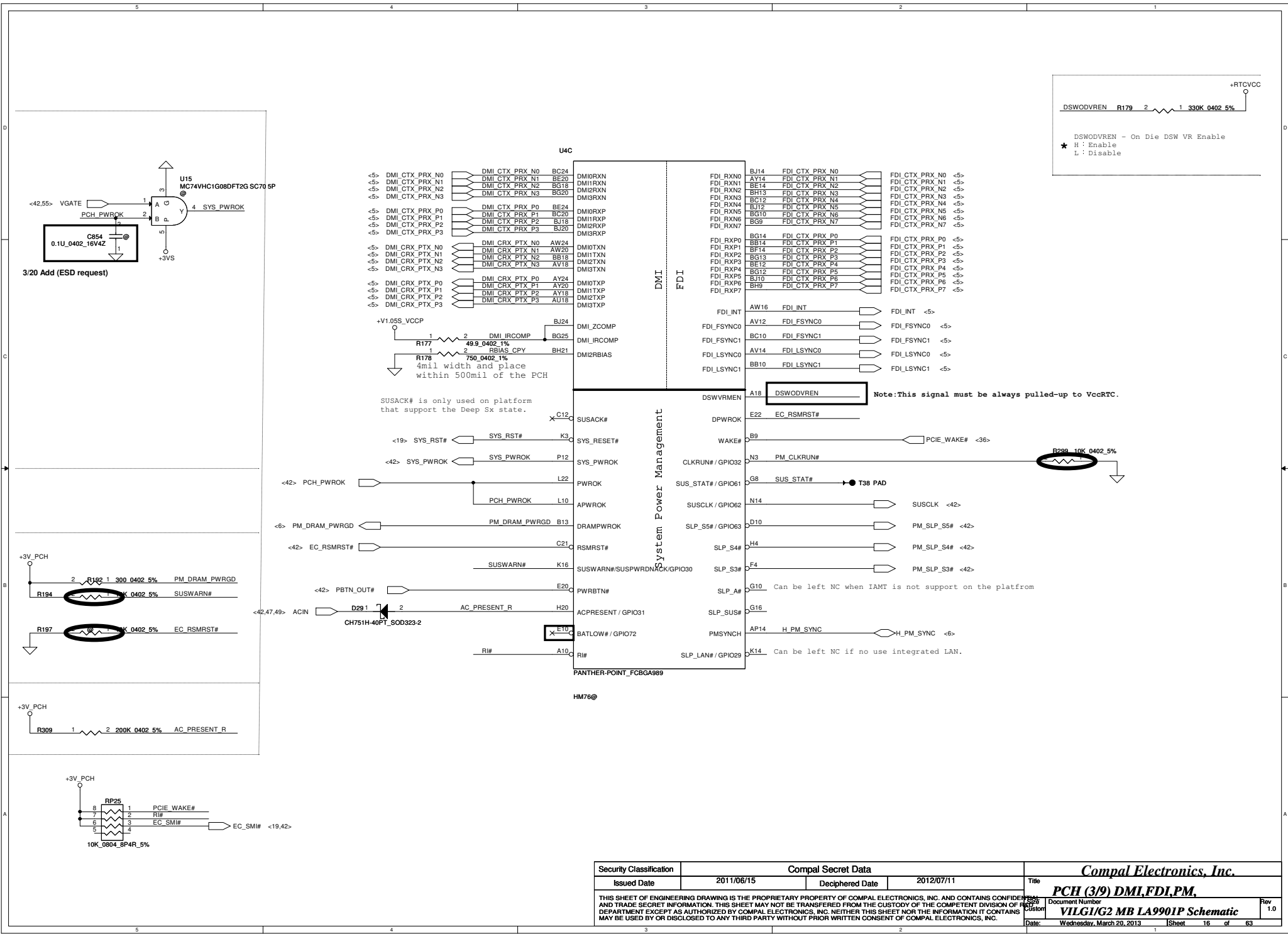
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|---|---------------------------|-----------------|------------|---|
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| Size | Custom | Document Number | VILG1/G2 MB LA9901P Schematic | | Rev 1.0 |
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| PCH (2)9 PCIE, SMBUS, CLK | | | | VILGI/G2 MB LA9901P Schematic |
| Date: Wednesday, March 20, 2013 | | | | Rev 1.0 |



DSWODVREN R179 2 1 330K 0402 5% +RTCVCC

DSWODVREN - On Die DSW VR Enable
★ H : Enable
L : Disable

3/20 Add (ESD request)

+3V_PCH

R194 1 300 0402 5% PM_DRAM_PWRGD

R197 1 300 0402 5% SUSWRN#

R197 1 300 0402 5% EC_RSMRST#

+3V_PCH

R309 1 200K 0402 5% AC_PRESENT_R

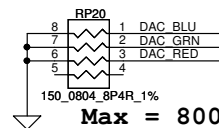
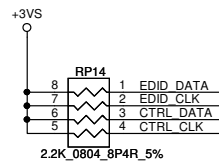
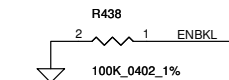
+3V_PCH

RP25 1 10K 0804 8P4R 5%

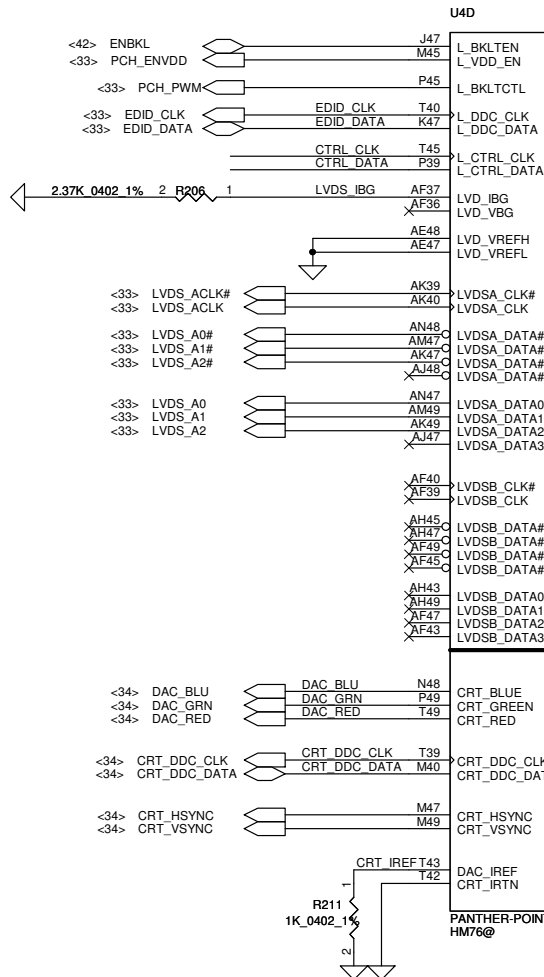
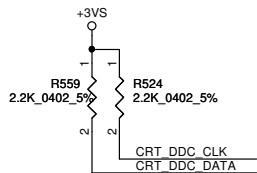
PCIE_WAKE#

EC_SM# <19,42>

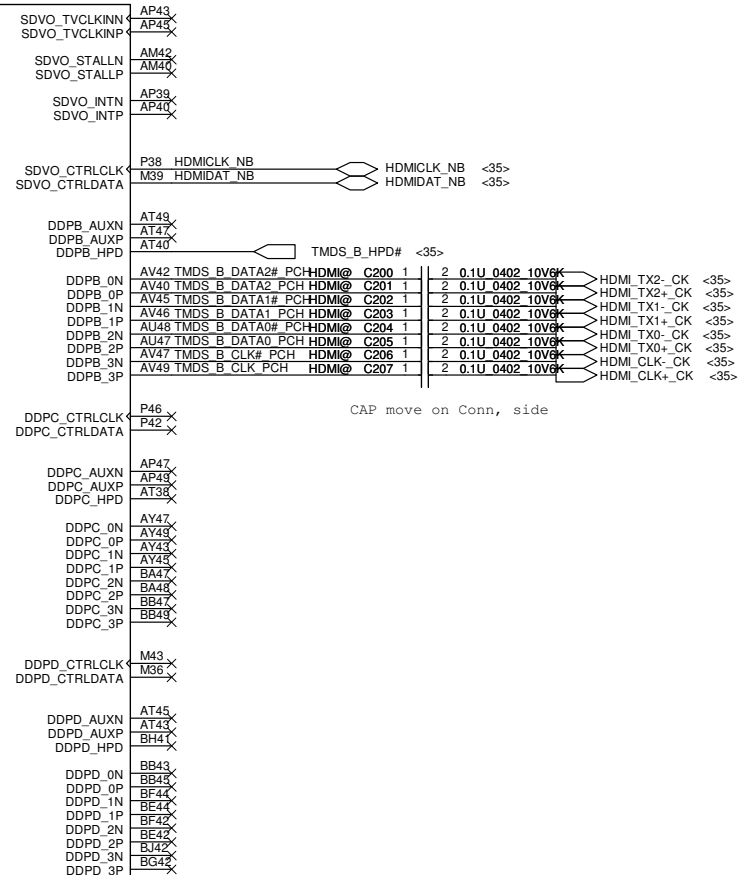
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|---|---------------------------|-----------------|-------------------------------|
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| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |
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| Rev | 1.0 | Document Number | VILG1/G2 MB LA9901P Schematic |
| Date: | Wednesday, March 20, 2013 | Sheet | 16 of 63 |



Max = 800 mils

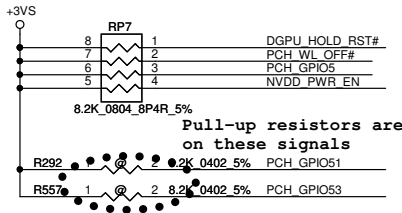
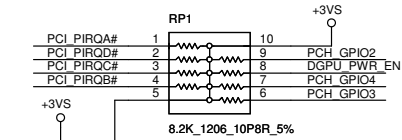


Digital Display Interface



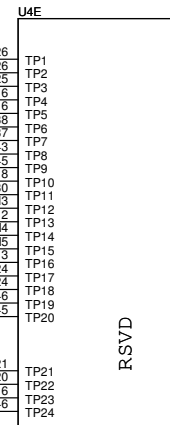
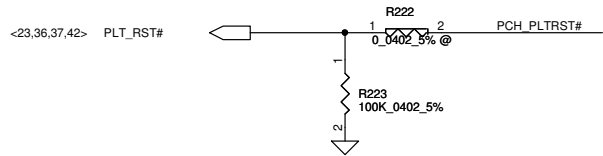
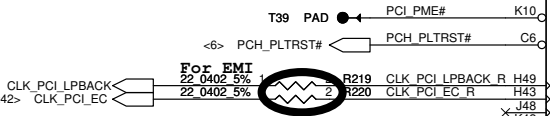
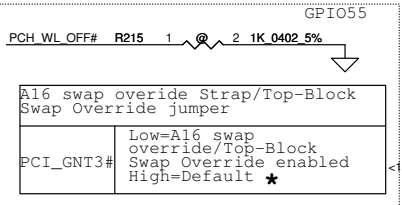
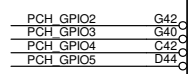
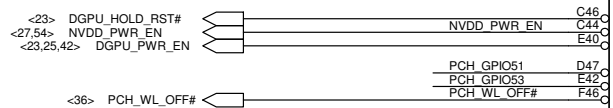
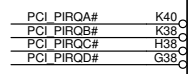
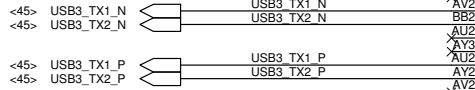
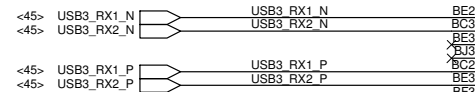
HDMI D2
HDMI D1
HDMI D0
HDMI CLK

| | | | | | | | | | |
|---|--|--------------------|--|-----------------|--|--------------------------|-------------------------------|----------------------------|-------|
| Security Classification | | Compal Secret Data | | | | Compal Electronics, Inc. | | | |
| Issued Date | | 2011/06/15 | | Deciphered Date | | 2012/07/11 | | Title | |
| | | | | | | | | PCH (4/9) LVDS,CRT,DP,HDMI | |
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| | | | | | | | VILG1/G2 MB LA9901P Schematic | | 1.0 |
| | | | | | | Date: | Wednesday, March 20, 2013 | | Sheet |



Pull-up resistors are not required on these signals

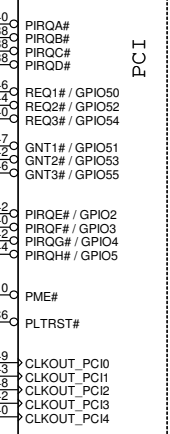
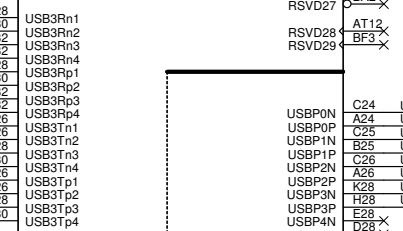
| Boot BIOS Strap | | | |
|--------------------|-----------------|-----------------|--------------------------|
| GNT1#/ GPIO51 | GPIO51 Bit11 | GPIO19 Bit10 | Boot BIOS Destination |
| SATA1GP/ GPIO19 | 0 | 1 | Reserved |
| Internal | 1 | 0 | PCI |
| PH | 0 | 0 | LPC |



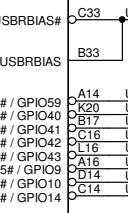
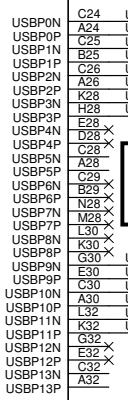
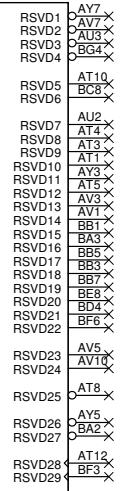
RSVD

PCI

USB



PANTHER-POINT_FCBGA389
HM76@

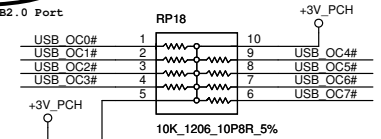
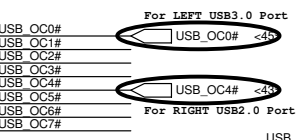


HM76 not support USB2.0 for port 6-7
HM70 not support USB2.0 for port 4-7 & 12 & 13
NM70 not support USB2.0 for port 4-7 & 12 & 13

USB DEBUG=PORT1 AND PORT9

LEFT USB (USB 3.0)
LEFT USB
Touch Screen
USB Camera

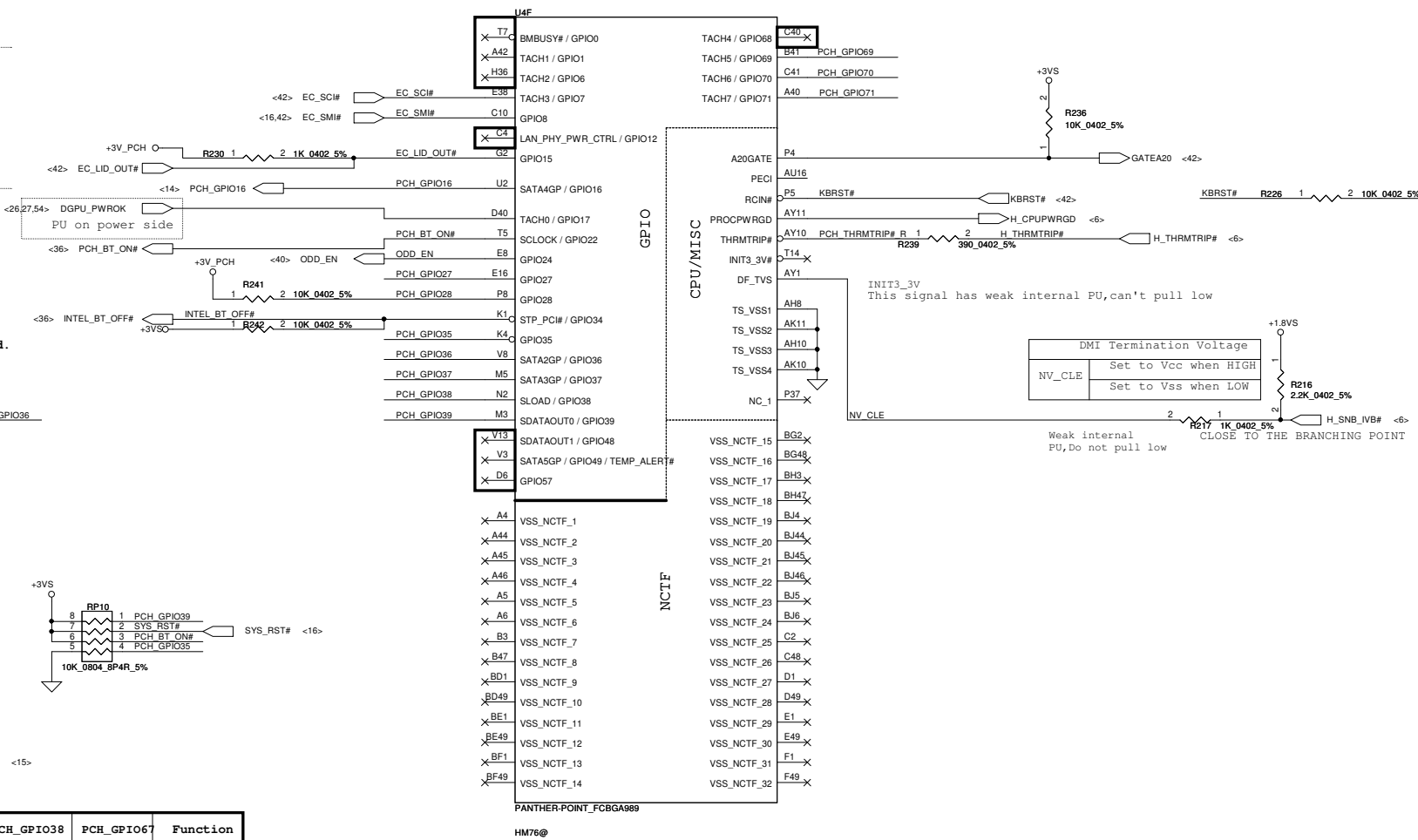
USB2.0
WLAN
CARD READER



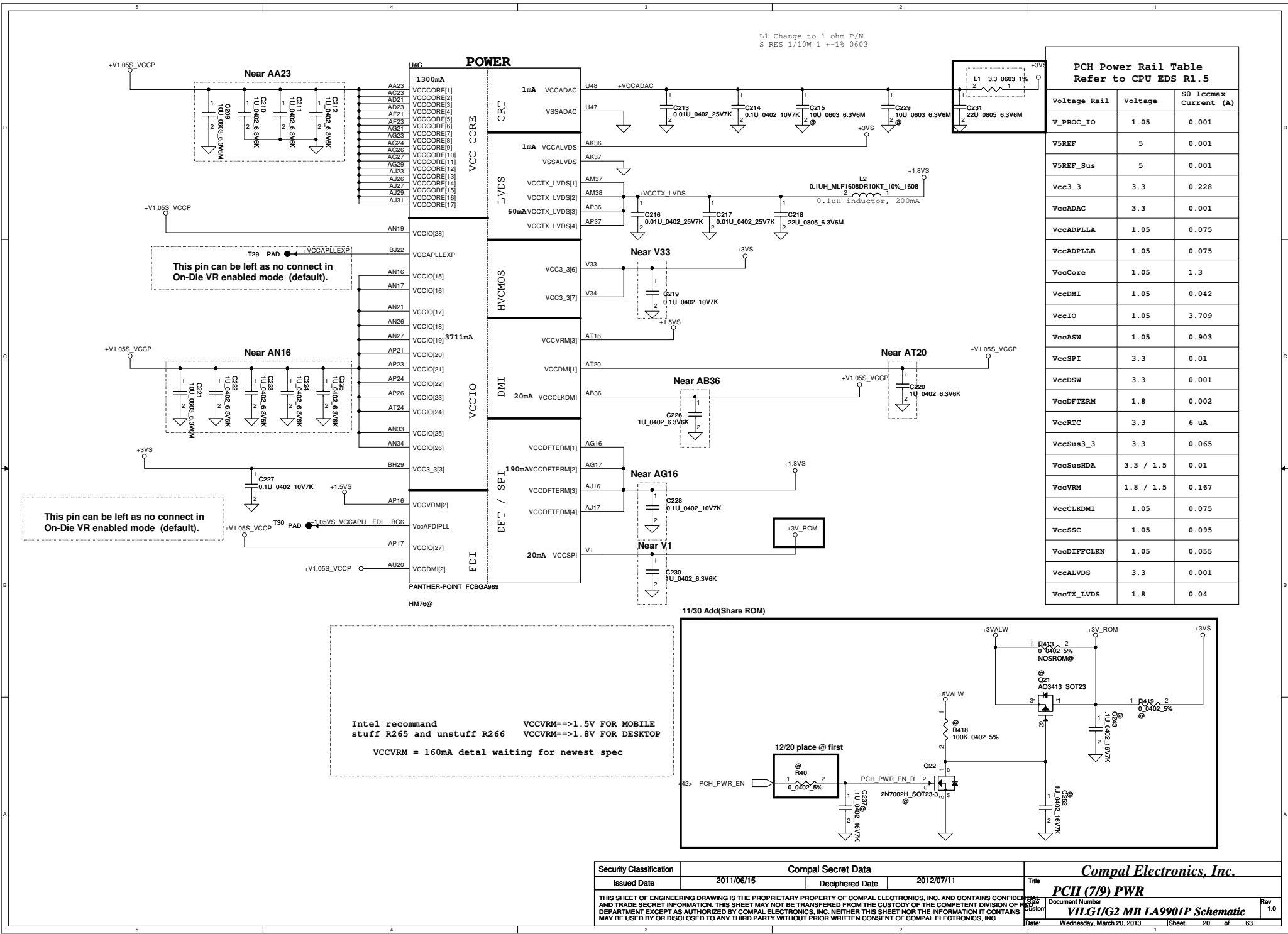
| | | | | | |
|--|--------------------|-----------------|------------|-------------------------------|----------|
| Security Classification | Compal Secret Data | | | Title | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 | PCH (5/9) PCI, USB | |
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| | | | | VILG1/G2 MB LA9901P Schematic | 1.0 |
| | | | | Date | Sheet |
| | | | | Wednesday, March 20, 2013 | 18 of 63 |

[illegible]

The diagram shows the RP10 module connected to a 3V5 supply. The module's pins are connected as follows: pin 8 to 3V5, pin 7 to 3V5, pin 6 to 3V5, and pin 5 to 3V5. Pin 1 is connected to PCH GPIO39, pin 2 to SYS_RST#, pin 3 to PCH BT_ON#, and pin 4 to PCH GPIO35. The output of the resistor network is labeled SYS_RST# <16>.

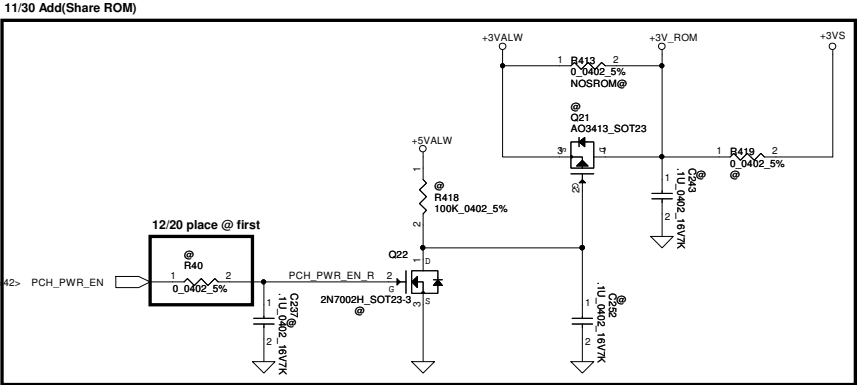


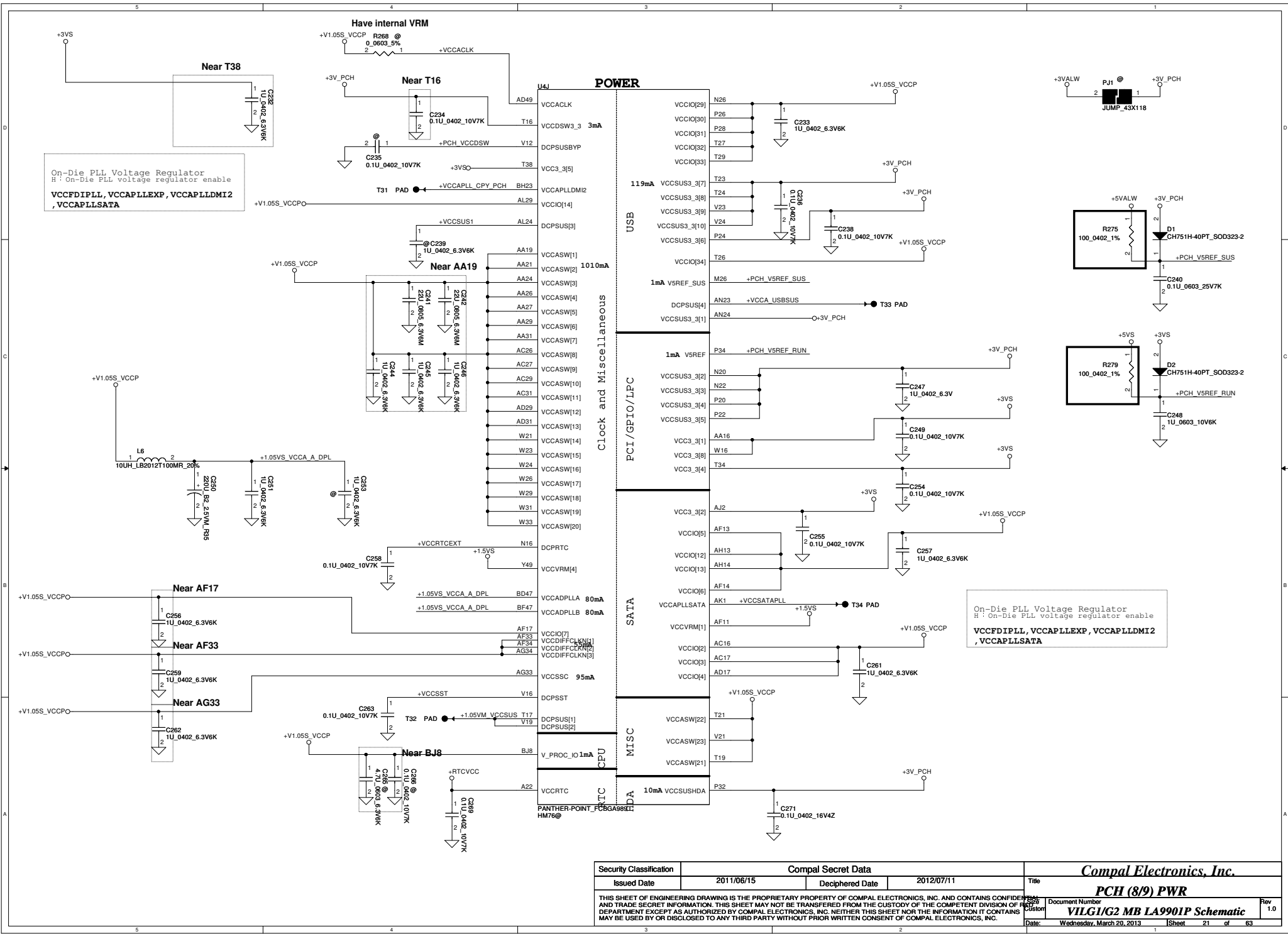
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|---|------------|--------------------|------------|---------------------------------|--|-------|----------|
| Security Classification | | Compal Secret Data | | <i>Compal Electronics, Inc.</i> | | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 | Title | <i>PCH (69) GPIO, CPU, MISC</i> | | |
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| | | | | Doc Name | VILG1/G2 MB LA9901P Schematic | | 1.0 |
| | | | | Date: | Wednesday, March 20, 2013 | Sheet | 19 of 63 |

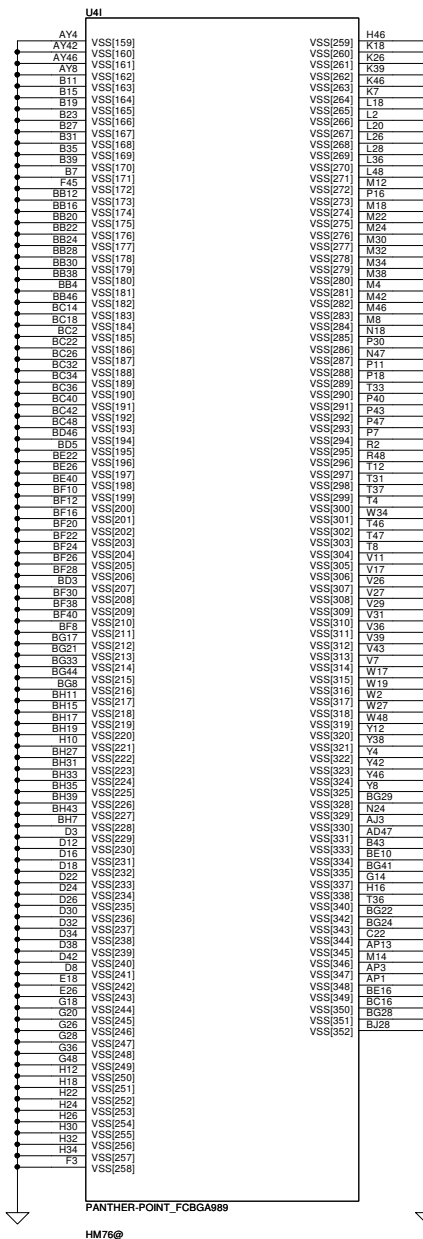


L1 Change to 1 ohm P/N
S RES 1/10W 1 +/-1% 0603

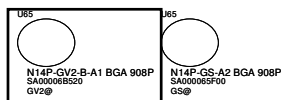
| PCH Power Rail Table Refer to CPU EDS R1.5 | | |
|---|-----------|-----------------------|
| Voltage Rail | Voltage | S0 Iccmax Current (A) |
| V_PROC_IO | 1.05 | 0.001 |
| V5REF | 5 | 0.001 |
| V5REF_Sus | 5 | 0.001 |
| Vcc3_3 | 3.3 | 0.228 |
| VccADAC | 3.3 | 0.001 |
| VccADPLLA | 1.05 | 0.075 |
| VccADPLLB | 1.05 | 0.075 |
| VccCore | 1.05 | 1.3 |
| VccDMI | 1.05 | 0.042 |
| VccIO | 1.05 | 3.709 |
| VccASW | 1.05 | 0.903 |
| VccSPI | 3.3 | 0.01 |
| VccDSW | 3.3 | 0.001 |
| VccDFTerm | 1.8 | 0.002 |
| VccRTC | 3.3 | 6 uA |
| VccSus3_3 | 3.3 | 0.065 |
| VccSusHDA | 3.3 / 1.5 | 0.01 |
| VccVRM | 1.8 / 1.5 | 0.167 |
| VccCLKDMI | 1.05 | 0.075 |
| VccSSC | 1.05 | 0.095 |
| VccDIFFCLKN | 1.05 | 0.055 |
| VccALVDS | 3.3 | 0.001 |
| VccTX_LVDS | 1.8 | 0.04 |





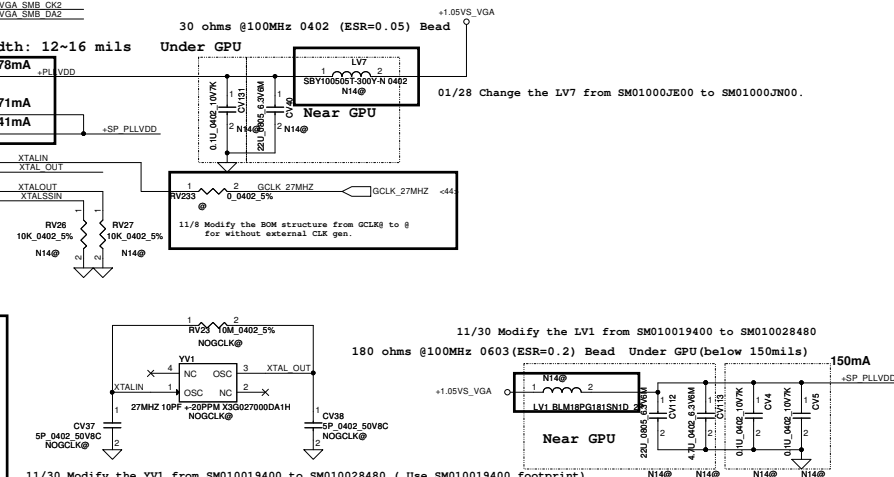
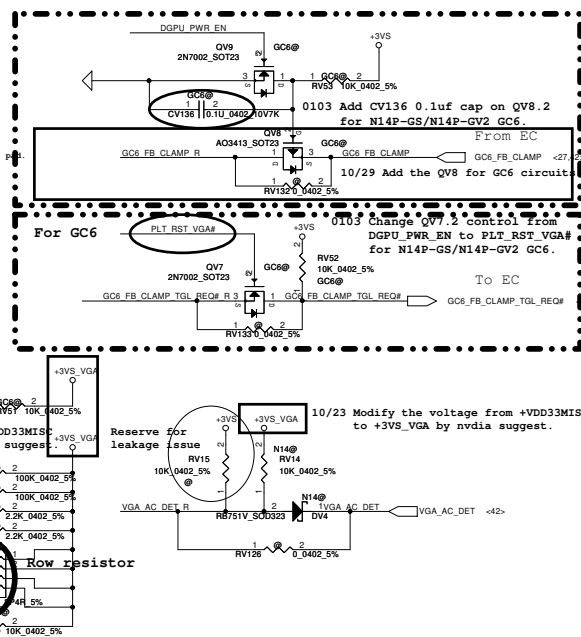
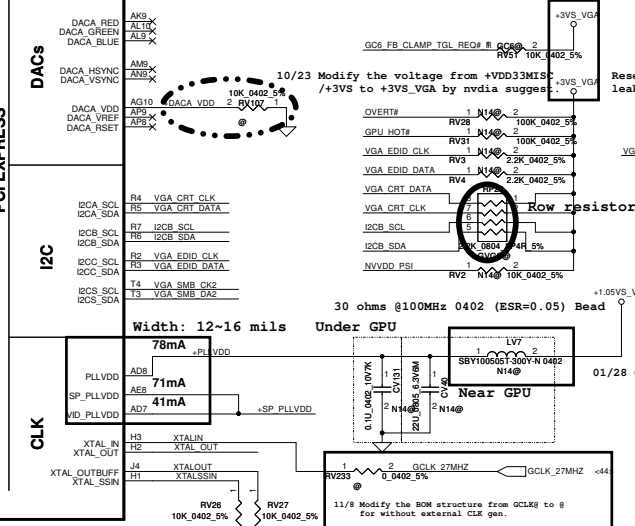
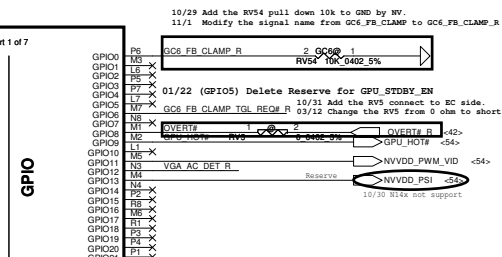
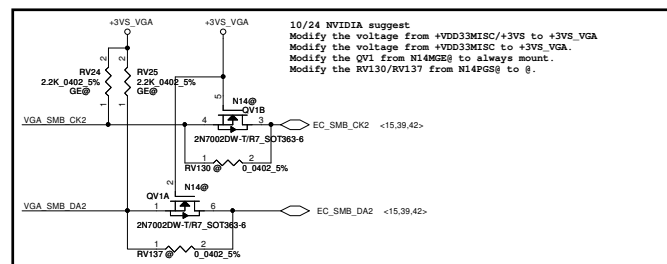
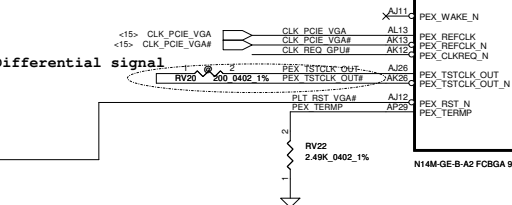
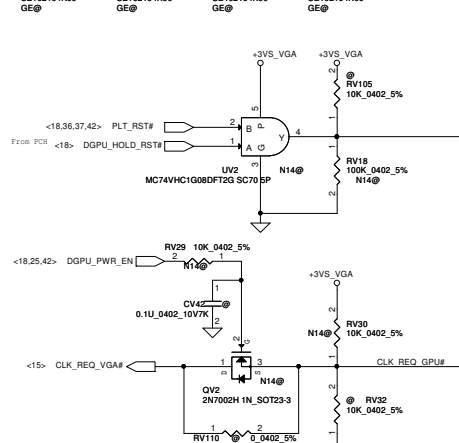
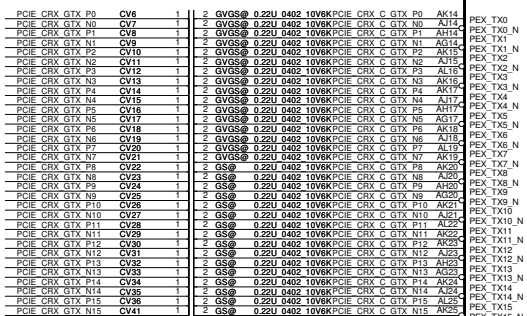
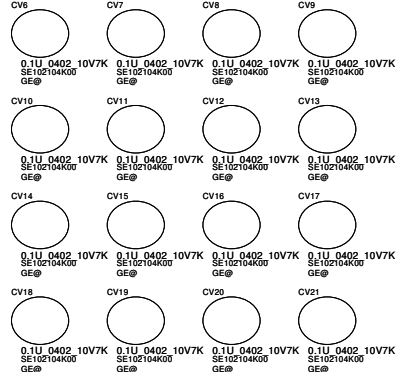


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|--|--|--------------------|-----------------|-------------------------------|---------------------------|-------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | | |
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| | | | | Title | PCH (9/9) VSS | |
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| | | | | VILG1/G2 MB LA9901P Schematic | | 1.0 |
| | | | | Date | Wednesday, March 20, 2013 | Sheet |



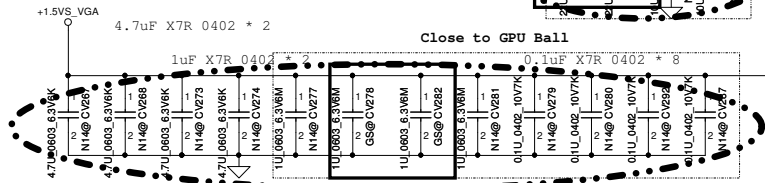
Non-support PCIE port8-15:N14M-GM and N14P-GV2

Support PCIe port8-15:N14P-GS



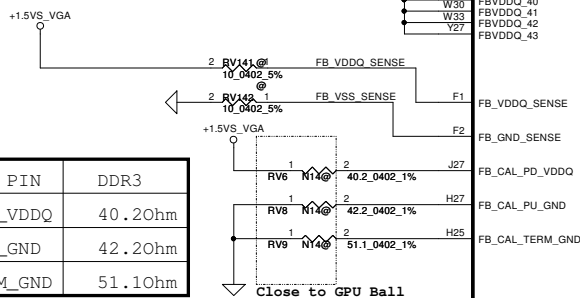
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| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. NI14X-PCIE/DAC/GPIO | |
| Issued Date | 2011/06/15 | Declassified Date | 2012/07/11 | Title | NI14X-PCIE/DAC/GPIO VIL7G/2 MB LA-9901P 3 |
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| | | | | Date | Wednesday, 2013. 03. 27 13:04:00 |

0128: Change the BOM structure of CV58/CV59/CV278/CV282 from N14@ to GS@.

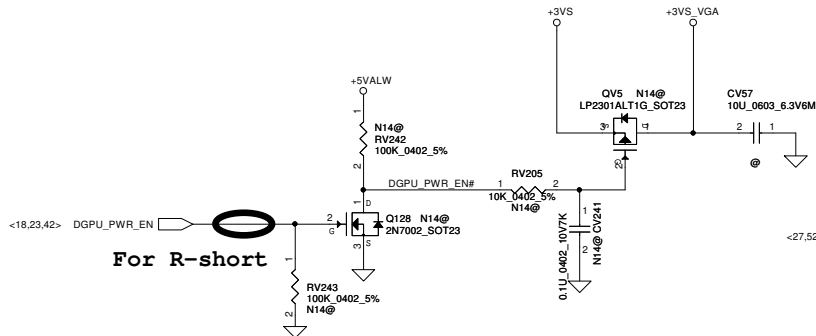


rise 1.5v system source voltage to 1.55-1.57V

| | |
|-------------------|---------|
| CALIBRATION PIN | DDR3 |
| FB_CAL_x_PD_VDDQ | 40.2ohm |
| FB_CAL_x_PU_GND | 42.2ohm |
| FB_CAL_x_TERM_GND | 51.1ohm |



+3VS to +3VS_VGA



For R-short

POWER

N14M-GE-S-A2 FGBGA 908P

Row resistor

Part 5 of 7

AA27 FBVDDQ_0
AA30 FBVDDQ_1
AB27 FBVDDQ_2
AB33 FBVDDQ_3
AC27 FBVDDQ_4
AD27 FBVDDQ_5
AE27 FBVDDQ_6
AF27 FBVDDQ_7
AG27 FBVDDQ_8
B13 FBVDDQ_9
B16 FBVDDQ_10
B19 FBVDDQ_11
E13 FBVDDQ_12
E16 FBVDDQ_13
E19 FBVDDQ_14
H10 FBVDDQ_15
H11 FBVDDQ_16
H12 FBVDDQ_17
H13 FBVDDQ_18
H14 FBVDDQ_19
H15 FBVDDQ_20
H16 FBVDDQ_21
H18 FBVDDQ_22
H20 FBVDDQ_23
H21 FBVDDQ_24
H22 FBVDDQ_25
H23 FBVDDQ_26
H24 FBVDDQ_27
H8 FBVDDQ_28
H9 FBVDDQ_29
H127 FBVDDQ_30
M27 FBVDDQ_31
N27 FBVDDQ_32
P27 FBVDDQ_33
R27 FBVDDQ_34
T27 FBVDDQ_35
T30 FBVDDQ_36
T33 FBVDDQ_37
V27 FBVDDQ_38
W27 FBVDDQ_39
W30 FBVDDQ_40
W33 FBVDDQ_41
Y27 FBVDDQ_42
Y27 FBVDDQ_43

PEX_IOVDD_0
PEX_IOVDD_1
PEX_IOVDD_2
PEX_IOVDD_3
PEX_IOVDD_4
PEX_IOVDD_5
AG19
AG21
AG22
AG24
AH21
AH25
AG13
AG15
AG16
AG18
AG25
AG26
AH15
AH18
AH28
AJ27
AK27
AL27
AM28
AN28

PEX_PLL_HVDD

210mA

PEX_SVDD_3V3

PEX_PLLVDD

VDD33_0
VDD33_1
VDD33_2
VDD33_3

IFPAB_PLLVDD

IFPAB_RSET

IFPA_IOVDD

IFPB_IOVDD

IFPC_PLLVDD

IFPC_RSET

IFPD_PLLVDD

IFPD_RSET

IFPE_PLLVDD

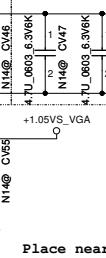
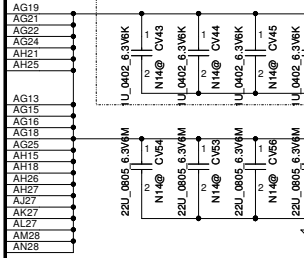
IFPE_RSET

IFPE_IOVDD

IFPF_IOVDD

3300mA Under GPU (below 150mils)

Near GPU



Place near balls

RV143

0.0603_5%

11/29 Modify the RV138 from 0ohm to short pad.

RV143

0.0603_5%

RV143

0.0603_5%

RV143

0.0603_5%

RV143

0.0603_5%

RV143

0.0603_5%

RV143

0.0603_5%

RV143

0.0603_5%

RV143

0.0603_5%

RV143

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RV143

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RV143

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RV143

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RV143

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RV143

0.0603_5%

RV143

0.0603_5%

RV143

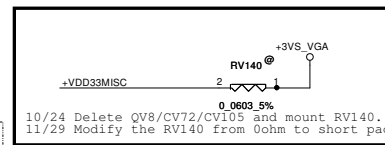
0.0603_5%

RV143

0.0603_5%

RV143

0.0603_5%



10/24 Delete QV8/CV72/CV105 and mount RV140.

11/29 Modify the RV140 from 0ohm to short pad.

RV140

0.0603_5%

RV140

0.0603_5%

RV140

0.0603_5%

RV140

0.0603_5%

RV140

0.0603_5%

RV140

0.0603_5%

RV140

0.0603_5%

RV140

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RV140

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RV140

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RV140

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RV140

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RV140

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RV140

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RV140

0.0603_5%

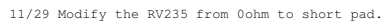
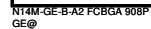
RV140

0.0603_5%

RV140

0.0603_5%

| | | | |
|--|---------------------------|-----------------|------------|
| Security Classification | Compal Secret Data | Document Number | N14X-POWER |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |
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| Date: | Wednesday, March 20, 2013 | Sheet | 25 of 63 |



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|--|--|--------------------|-----------------|---------------------------------|--------------------------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | | 2011/06/15 | Deciphered Date | | 2012/07/11 |
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| | | | | Document Number | VILG1/G2 MB LA-9901P Schematic |
| | | | | Date: Wednesday, March 20, 2013 | Sheet 26 of 63 |
| | | | | Rev | 0.3 |

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FBA_D62 M90 FBA_D62
FBA_D63 M91 FBA_D63

Part 2 of 7
MEMORY INTERFACE
A

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FBA_CMD1 M30 FBA_CMD1
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FBA_CMD3 M32 FBA_CMD3
FBA_CMD4 M33 FBA_CMD4
FBA_CMD5 M34 FBA_CMD5
FBA_CMD6 M35 FBA_CMD6
FBA_CMD7 M36 FBA_CMD7
FBA_CMD8 M37 FBA_CMD8
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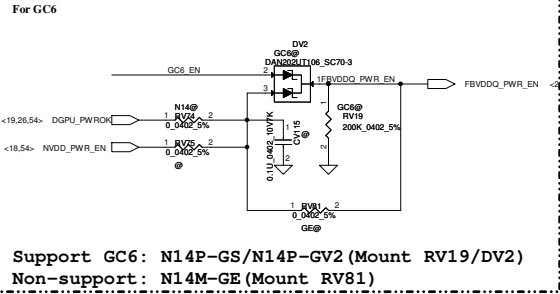
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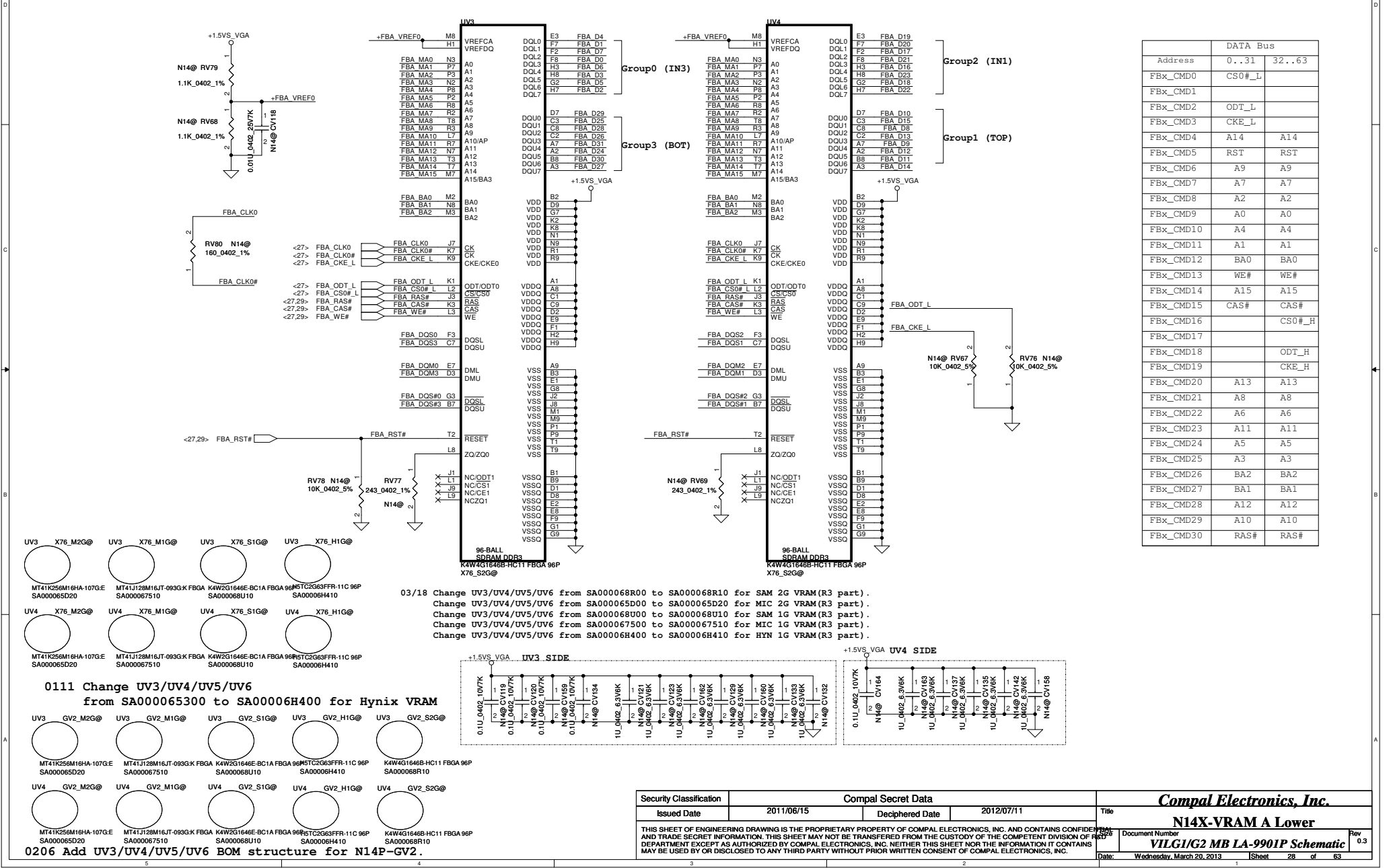
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| FbxC_CMD3 RST | |
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| FbxC_CMD5 A9 | A9 |
| FbxC_CMD6 A7 | A7 |
| FbxC_CMD7 A2 | A2 |
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| FbxC_CMD9 A4 | A4 |
| FbxC_CMD10 A1 | A1 |
| FbxC_CMD11 BA0 | BA0 |
| FbxC_CMD12 WE# | WE# |
| FbxC_CMD13 A15 | A15 |
| FbxC_CMD14 CAS# | CAS# |
| FbxC_CMD15 CS0#_H | |
| FbxC_CMD16 ODT_H | |
| FbxC_CMD17 CKE_H | |
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| FbxC_CMD19 A8 | A8 |
| FbxC_CMD20 A6 | A6 |
| FbxC_CMD21 A11 | A11 |
| FbxC_CMD22 A5 | A5 |
| FbxC_CMD23 A3 | A3 |
| FbxC_CMD24 BA2 | BA2 |
| FbxC_CMD25 BA1 | BA1 |
| FbxC_CMD26 A12 | A12 |
| FbxC_CMD27 A10 | A10 |
| FbxC_CMD28 A5# | A5# |



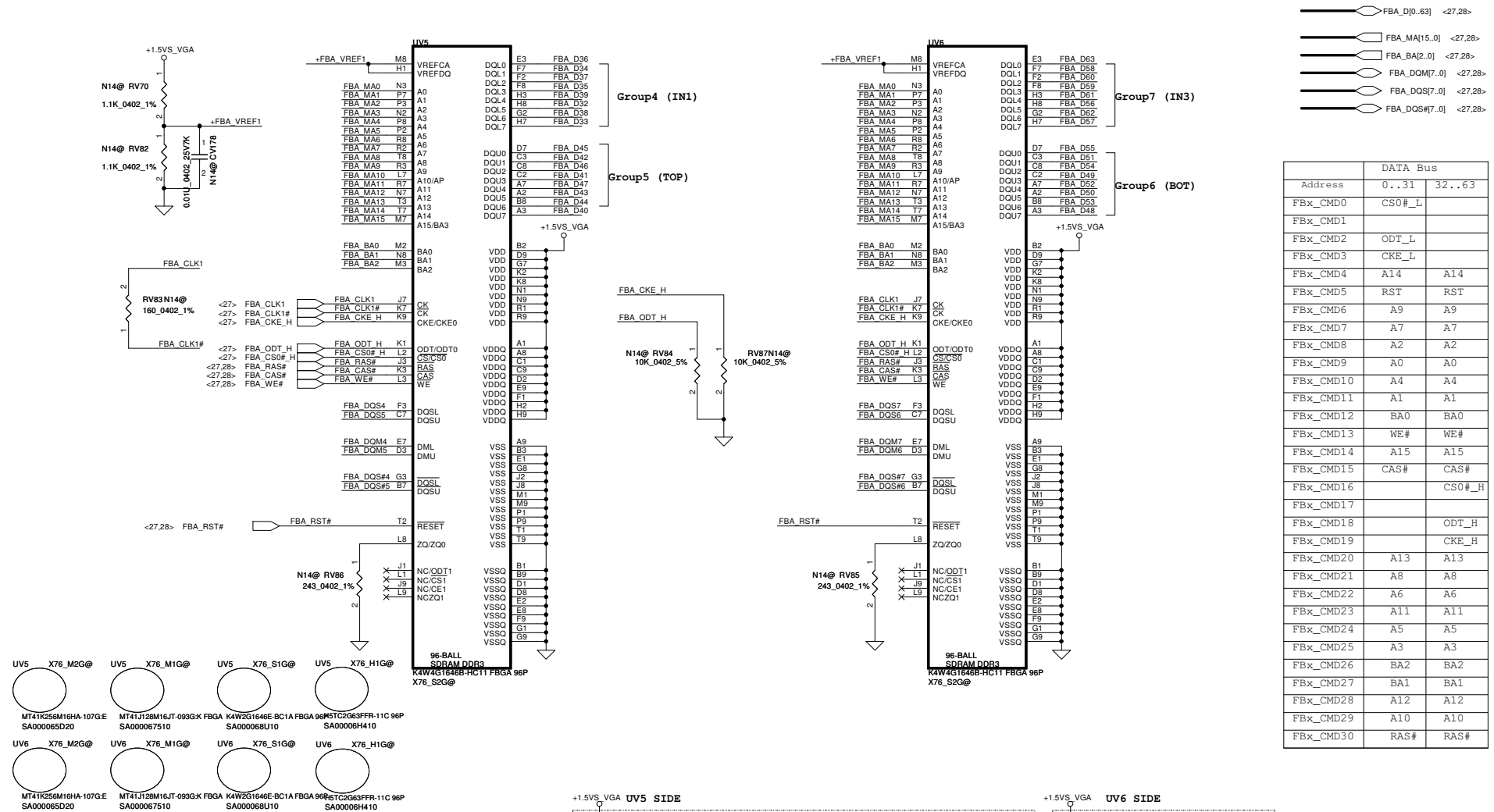
Support GC6: N14P-GS/N14P-GV2 (Mount RV19/DV2)
Non-support: N14M-GE (Mount RV81)

| Security Classification | Compal Secret Data | Document Number |
|-------------------------|--------------------|-----------------|
|-------------------------|--------------------|-----------------|

Memory Partition A - Lower 32 bits



Memory Partition A - Upper 32 bits



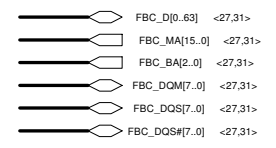
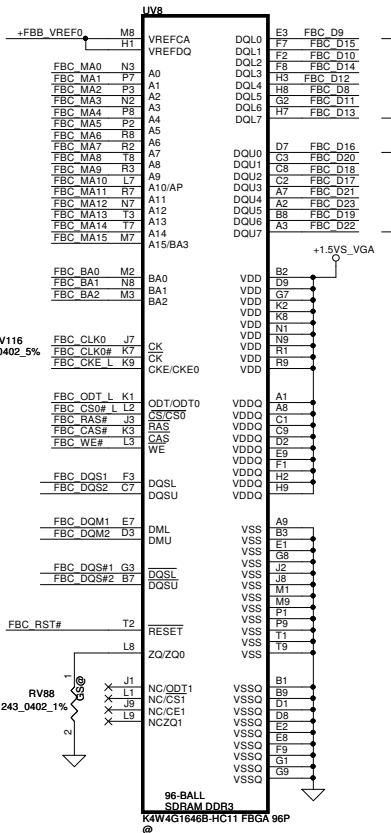
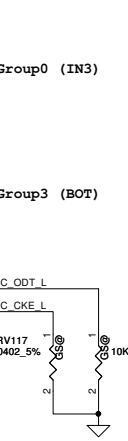
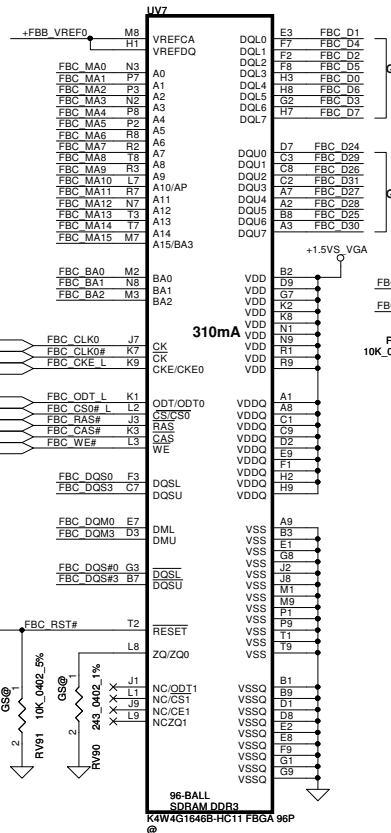
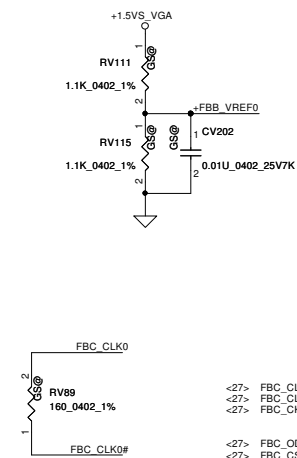
| Address | DATA Bus |
|-----------|----------|
| FBx_CMD0 | CS0#_L |
| FBx_CMD1 | |
| FBx_CMD2 | ODT_L |
| FBx_CMD3 | CKE_L |
| FBx_CMD4 | A14 |
| FBx_CMD5 | RST |
| FBx_CMD6 | A9 |
| FBx_CMD7 | A7 |
| FBx_CMD8 | A2 |
| FBx_CMD9 | A0 |
| FBx_CMD10 | A4 |
| FBx_CMD11 | A1 |
| FBx_CMD12 | BA0 |
| FBx_CMD13 | WE# |
| FBx_CMD14 | A15 |
| FBx_CMD15 | CAS# |
| FBx_CMD16 | CS0#_H |
| FBx_CMD17 | |
| FBx_CMD18 | ODT_H |
| FBx_CMD19 | CKE_H |
| FBx_CMD20 | A13 |
| FBx_CMD21 | A8 |
| FBx_CMD22 | A6 |
| FBx_CMD23 | A11 |
| FBx_CMD24 | A5 |
| FBx_CMD25 | A3 |
| FBx_CMD26 | BA2 |
| FBx_CMD27 | BA1 |
| FBx_CMD28 | A12 |
| FBx_CMD29 | A10 |
| FBx_CMD30 | RAS# |

0111 Change UV3/UV4/UV5/UV6 from SA000065300 to SA00006H400 for Hynix VRAM

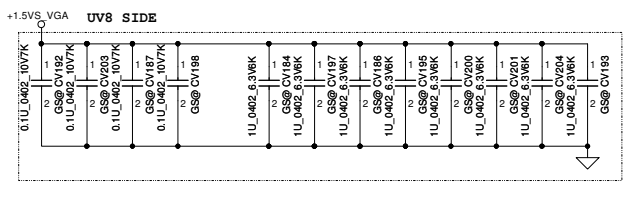
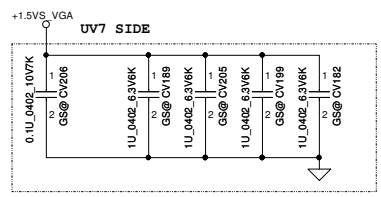
0206 Add UV3/UV4/UV5/UV6 BOM structure for N14P-GV2.

| Security Classification | Compal Secret Data | Title |
|--|--------------------|-------------------|
| Issued Date | Deciphered Date | Document Number |
| 2011/06/15 | 2012/07/11 | N14X-VRAM A Upper |
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| Date: Wednesday, March 20, 2013 | Sheet 29 of 63 | |

Memory Partition C - Lower 32 bits



| Address | DATA Bus |
|-----------|----------|
| FBx_CMD0 | CS0#_L |
| FBx_CMD1 | |
| FBx_CMD2 | ODT_L |
| FBx_CMD3 | CKE_L |
| FBx_CMD4 | A14 |
| FBx_CMD5 | RST |
| FBx_CMD6 | A9 |
| FBx_CMD7 | A7 |
| FBx_CMD8 | A2 |
| FBx_CMD9 | A0 |
| FBx_CMD10 | A4 |
| FBx_CMD11 | A1 |
| FBx_CMD12 | BA0 |
| FBx_CMD13 | WE# |
| FBx_CMD14 | A15 |
| FBx_CMD15 | CAS# |
| FBx_CMD16 | CS0#_H |
| FBx_CMD17 | |
| FBx_CMD18 | ODT_H |
| FBx_CMD19 | CKE_H |
| FBx_CMD20 | A13 |
| FBx_CMD21 | A8 |
| FBx_CMD22 | A6 |
| FBx_CMD23 | A11 |
| FBx_CMD24 | A5 |
| FBx_CMD25 | A3 |
| FBx_CMD26 | BA2 |
| FBx_CMD27 | BA1 |
| FBx_CMD28 | A12 |
| FBx_CMD29 | A10 |
| FBx_CMD30 | RAS# |

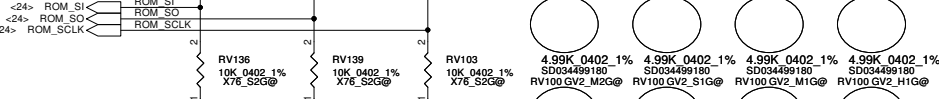
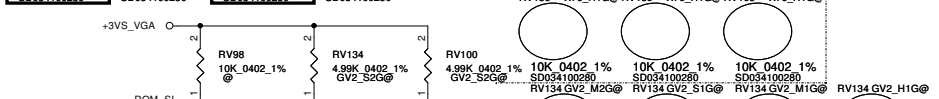
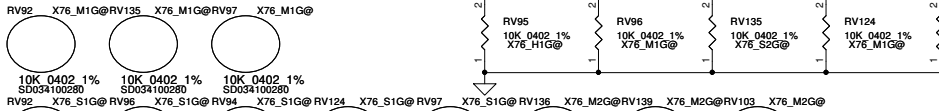


A

| | | | | | | |
|--|--------------------|-----------------|------------|---|---|----------------|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. N14X-VRAM C Upper | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 | Title | N14X-VRAM C Upper VILG1/G2 MB LA-9901P Schematic | |
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| | | | | Date: | Wednesday, March 20, 2013 | Sheet 31 of 63 |

N14M-GE X76

X7647138L01:X76_M2G@
X7647138L02:X76_S1G@
X7647138L03:X76_M1G@
X7647138L04:X76_S2G@
X7647138L05:X76_H1G@



For N14P-GV2 strap table X76

| GPU | Freq. | Memory Size | Memory Config | strap0 | strap1 | strap2 | strap3 | strap4 | ROM_SI | ROM_SO | ROM_SCLK |
|----------|---------|-------------|-----------------------------|--------|--------|--------|--------|--------|--------|--------|----------|
| N14P-GV2 | 1 GHz | 128M*16*4 | Samsung K4W2G1646E-BC1A | R | R | R | R | R | R | R | R |
| N14P-GV2 | 1 GHz | 128M*16*4 | Micron MT41J128M16JT-093G-K | R | R | R | R | R | R | R | R |
| N14P-GV2 | 1 GHz | 128M*16*4 | Hynix H5TC2G63FFR-11C | R | R | R | R | R | R | R | R |
| N14P-GV2 | 900 MHz | 256M*16*4 | Samsung K4W4G1646B-HC11 | R | R | R | R | R | R | R | R |
| N14P-GV2 | 900 MHz | 256M*16*4 | Micron MT41K256M16HA-107G-E | R | R | R | R | R | R | R | R |

For N14P-GS strap table X76

| GPU | Freq. | Memory Size | Memory Config | strap0 | strap1 | strap2 | strap3 | strap4 | ROM_SI | ROM_SO | ROM_SCLK |
|---------|---------|-------------|-----------------------------|--------|--------|--------|--------|--------|--------|--------|----------|
| N14P-GS | 1 GHz | 128M*16*8 | Samsung K4W2G1646E-BC1A | R | R | R | R | R | R | R | R |
| N14P-GS | 1 GHz | 128M*16*8 | Micron MT41J128M16JT-093G-K | R | R | R | R | R | R | R | R |
| N14P-GS | 1 GHz | 128M*16*8 | Hynix H5TC2G63FFR-11C | R | R | R | R | R | R | R | R |
| N14P-GS | 900 MHz | 256M*16*8 | Samsung K4W4G1646B-HC11 | R | R | R | R | R | R | R | R |
| N14P-GS | 900 MHz | 256M*16*8 | Micron MT41K256M16HA-107G-E | R | R | R | R | R | R | R | R |

For N14M-GE strap table X76

| GPU | Freq. | Memory Size | Memory Config | strap0 | strap1 | strap2 | strap3 | strap4 | ROM_SI | ROM_SO | ROM_SCLK |
|---------|---------|-------------|-----------------------------|--------|--------|--------|--------|--------|--------|--------|----------|
| N14M-GE | 1 GHz | 128M*16*4 | Samsung K4W2G1646E-BC1A | R | R | R | R | R | R | R | R |
| N14M-GE | 1 GHz | 128M*16*4 | Micron MT41J128M16JT-093G-K | R | R | R | R | R | R | R | R |
| N14M-GE | 1 GHz | 128M*16*4 | Hynix H5TC2G63FFR-11C | R | R | R | R | R | R | R | R |
| N14M-GE | 900 MHz | 256M*16*4 | Samsung K4W4G1646B-HC11 | R | R | R | R | R | R | R | R |
| N14M-GE | 900 MHz | 256M*16*4 | Micron MT41K256M16HA-107G-E | R | R | R | R | R | R | R | R |

VRAM Part Number

| Freq. | Memory Size | Micron | Hynix | Samsung | Micron |
|---------|-------------|------------|-------------|------------|------------|
| 1 GHz | 128M*16*8 | SA00006U10 | SA00006H410 | SA00006R10 | SA00006S20 |
| 900 MHz | 256M*16*8 | | | | |

Multi-Level Mode

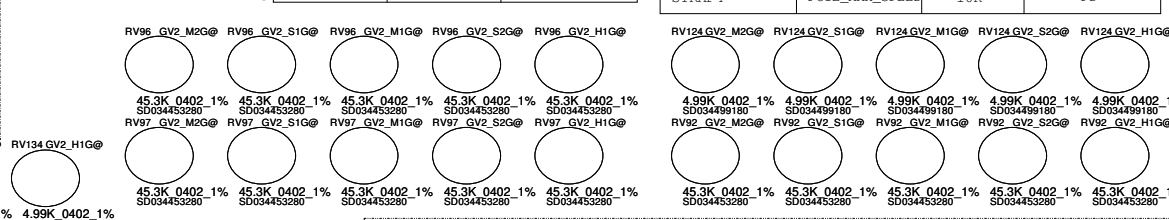
| Physical Strapping pin | Power Rail | Logical Strapping Bit3 | Logical Strapping Bit2 | Logical Strapping Bit1 | Logical Strapping Bit0 |
|------------------------|------------|------------------------|------------------------|------------------------|------------------------|
| ROM_SCLK | +3VS_VGA | PCI_DEVID[4] | SUB_VENDOR | SLOT_CLK_CFG | PEX_PLL_EN_TERM |
| ROM_SI | +3VS_VGA | RAM_CFG[3] | RAM_CFG[2] | RAM_CFG[1] | RAM_CFG[0] |
| ROM_SO | +3VS_VGA | FB[1] | FB[0] | SMB_ALT_ADDR | VGA_DEVICE |
| STRAP0 | +3VS_VGA | USER[3] | USER[2] | USER[1] | USER[0] |
| STRAP1 | +3VS_VGA | 3GIO_PADCFG[3] | 3GIO_PADCFG[2] | 3GIO_PADCFG[1] | 3GIO_PADCFG[0] |
| STRAP2 | +3VS_VGA | PCI_DEVID[3] | PCI_DEVID[2] | PCI_DEVID[1] | PCI_DEVID[0] |
| STRAP3 | +3VS_VGA | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED |
| STRAP4 | +3VS_VGA | RESERVED | PCIE_SPEED_CHANGE_GEN3 | PCIE_MAX_SPEED | DP_PLL_VDD33V |

Binary-Level Mode

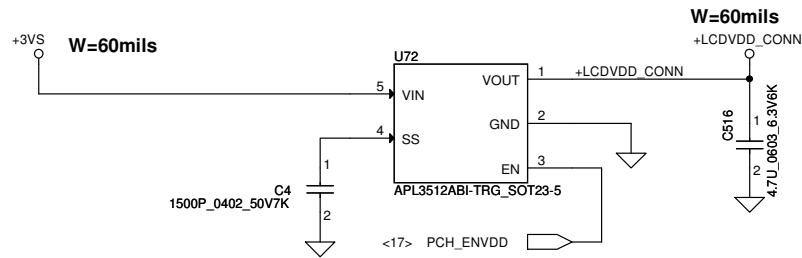
| Resistor Values | Pull-up to +3VS_VGA | Pull-down to Gnd | Physical Strapping pin | Strapping Mapping | Resistance | Polarity |
|-----------------|---------------------|------------------|------------------------|-------------------|------------|--------------------------------------|
| 4.99K | 1000 | 0000 | ROM_SCLK | SMB_ALT_ADDR | 10K | PD |
| 10.0K | 1001 | 0001 | ROM_SI | SUB_VENDOR | 10K | PU (VBIOS ROM) PD (Non-VBIOS ROM) |
| 15.0K | 1010 | 0010 | ROM_SO | VGA_DEVICE | 10K | PD (No display) |
| 20.0K | 1011 | 0011 | STRAP0 | RAM_CFG[0] | 10K | |
| 24.9K | 1100 | 0100 | STRAP1 | RAM_CFG[1] | 10K | PU (Binary=1) PD (Binary=0) |
| 30.1K | 1101 | 0101 | STRAP2 | RAM_CFG[2] | 10K | |
| 34.8K | 1110 | 0110 | STRAP3 | RAM_CFG[3] | 10K | |
| 45.3K | 1111 | 0111 | STRAP4 | PCIE_MAX_SPEED | 10K | PD |

N14P-GV2 X76

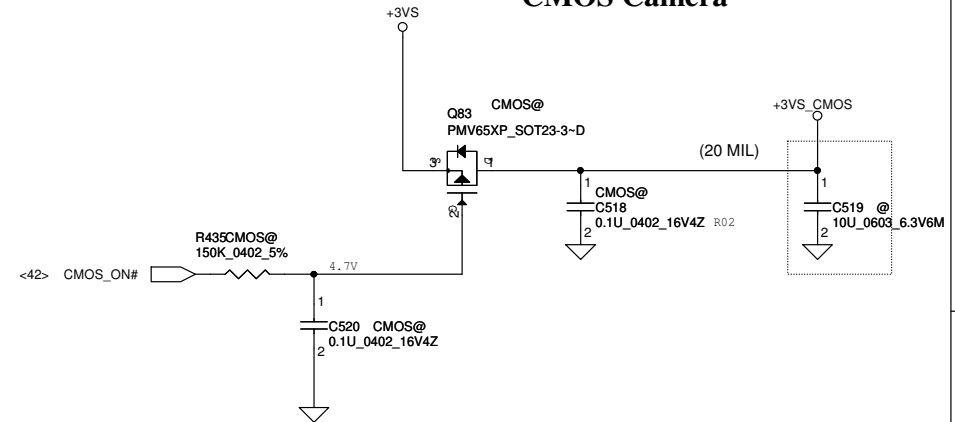
X7647138L06:GV2_M2G@
X7647138L07:GV2_S1G@
X7647138L08:GV2_M1G@
X7647138L09:GV2_S2G@
X7647138L10:GV2_H1G@



LCD POWER CIRCUIT

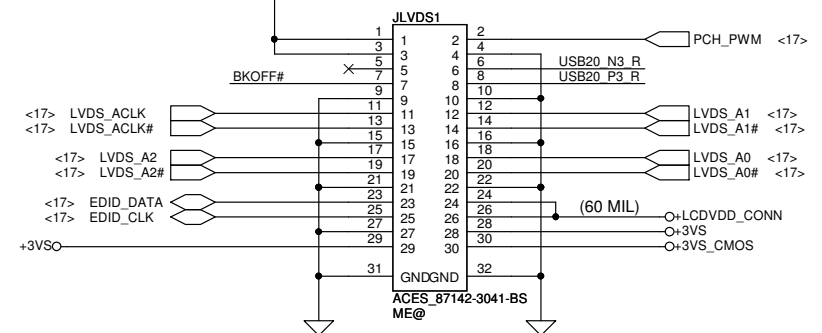
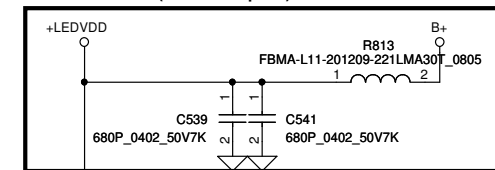


CMOS Camera

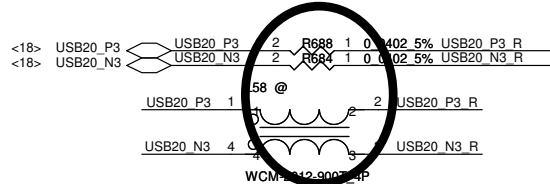


VGA LCD/PANEL BD. Conn.

12/12 Mount C539/C541 of 680pF, Chantage R813 to 220 ohm bead.(For EMI request)



For EMI



| | | | | | |
|---|--------------------|-----------------|------------|---------------------------------|-----------------|
| Security Classification | Compal Secret Data | | | Title | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 | Rev 1.0 | |
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| | | | | VILG1/G2 MB LA9901P Schematic | |
| | | | | Date: Wednesday, March 20, 2013 | Sheet 33 of 63 |

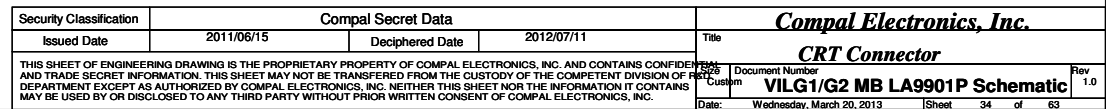
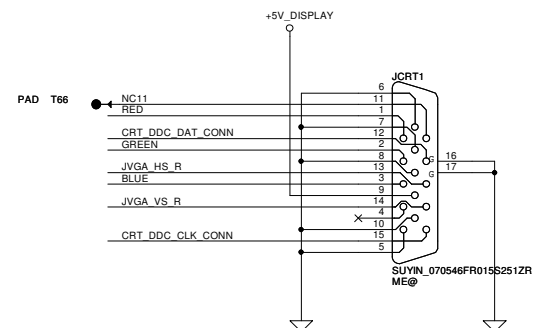
Compal Electronics, Inc.

LVDS/CAMERA

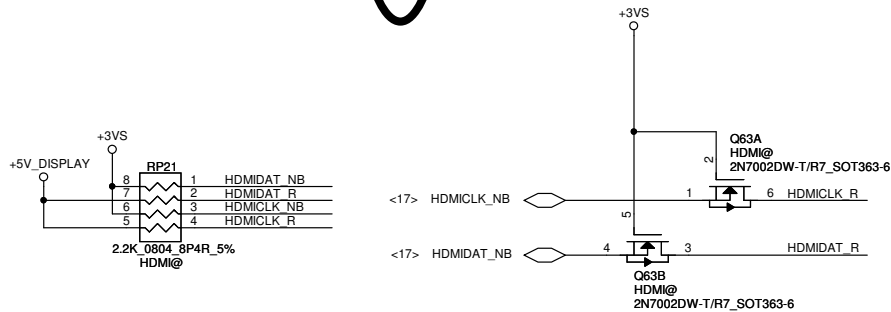
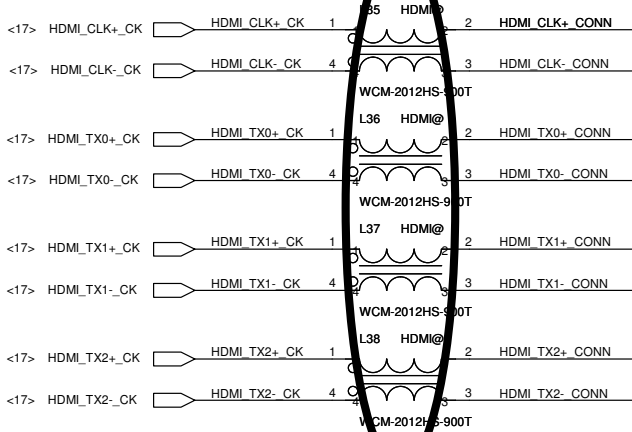
Size Custom Document Number

VILG1/G2 MB LA9901P Schematic

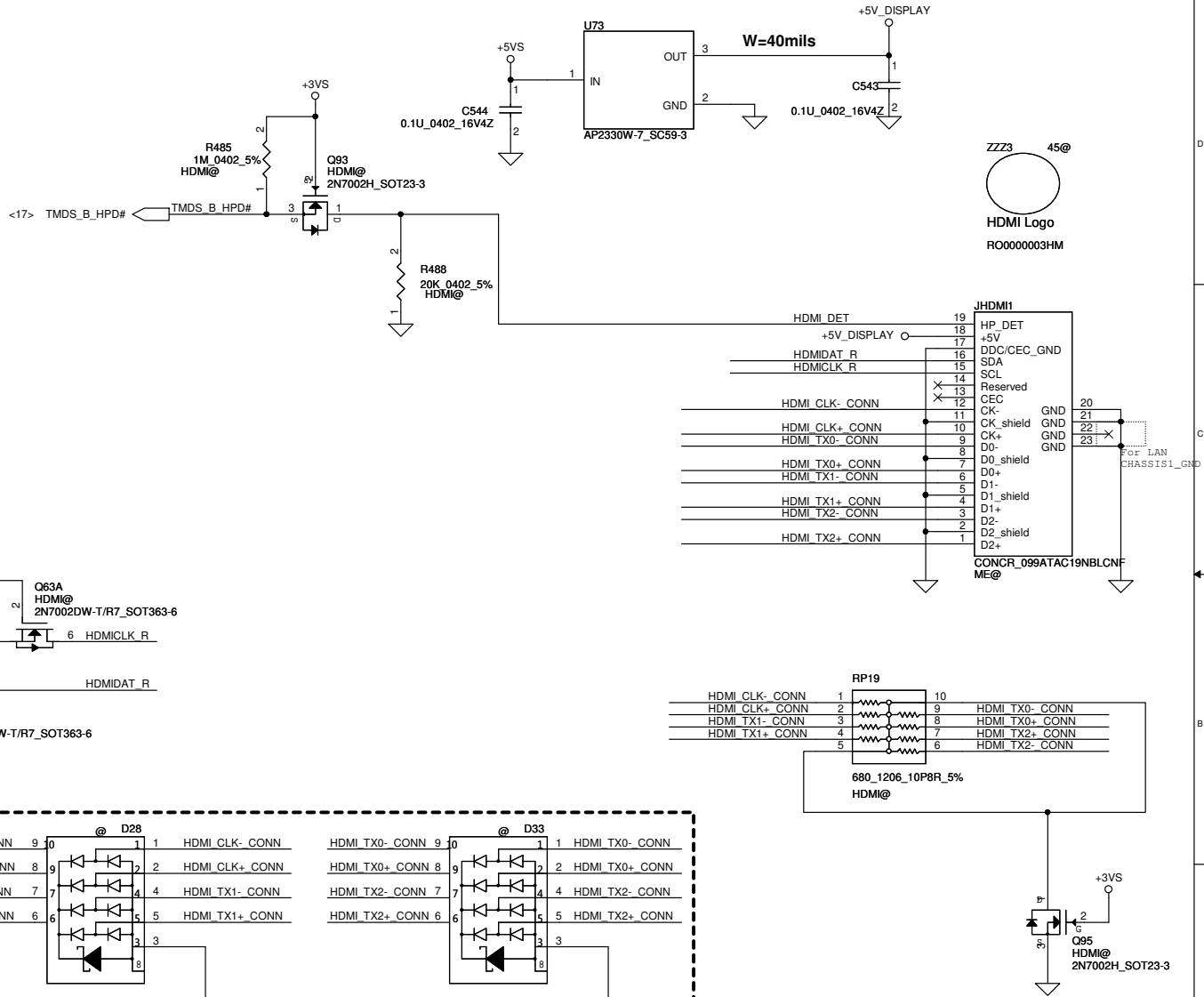
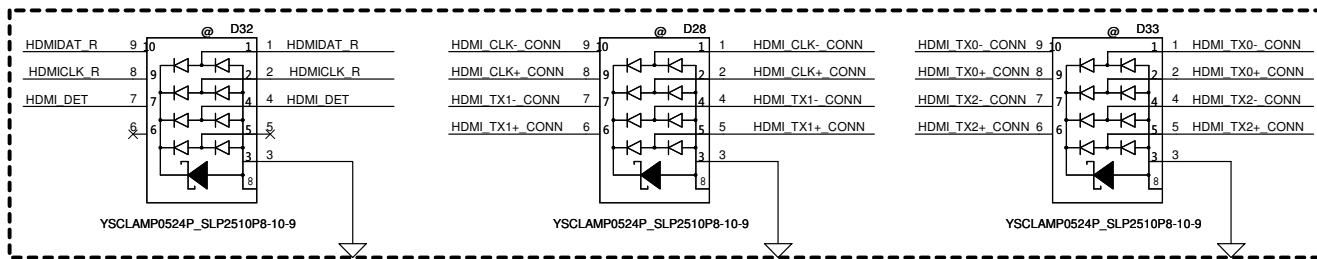
Date: Wednesday, March 20, 2013 Sheet 33 of 63



For EMI

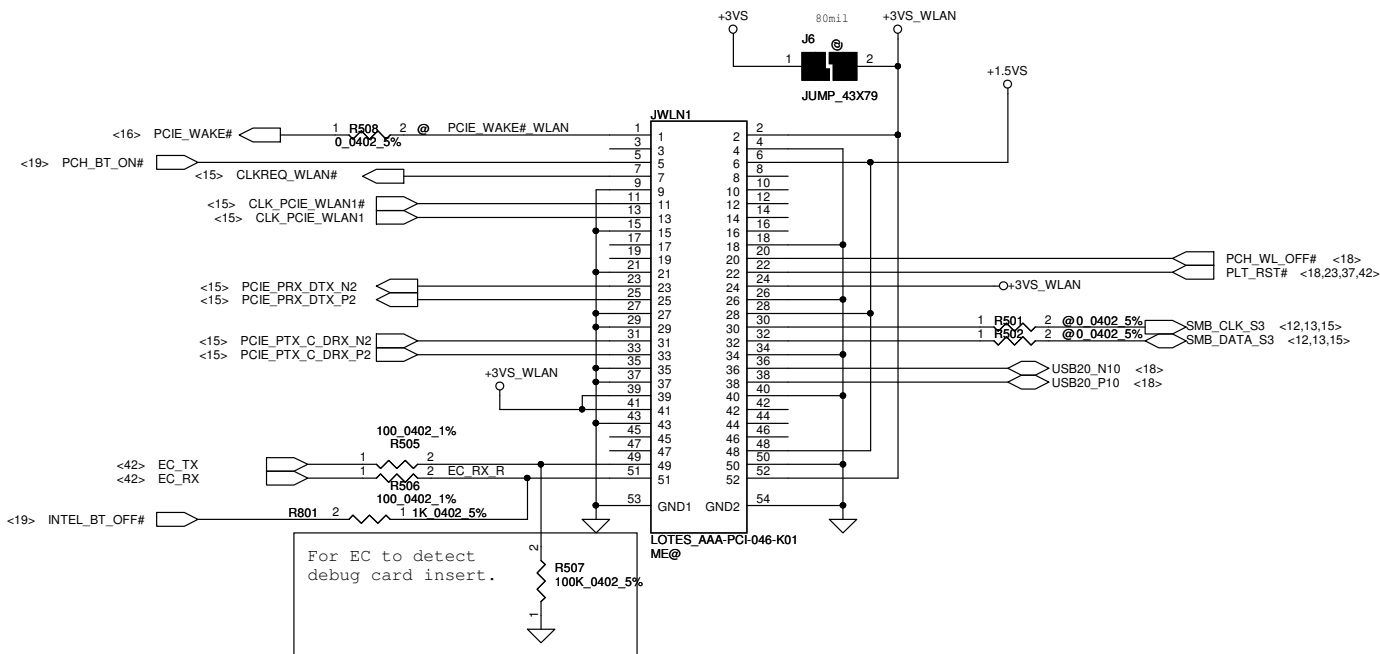


ESD



| | | | | | |
|---|------------|--------------------|------------|---------------------------------|-----------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 | Title | HDMI CONN |
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| | | | | VILG1/G2 MB LA9901P Schematic | |
| | | | | Date: Wednesday, March 20, 2013 | Sheet 35 of 63 |

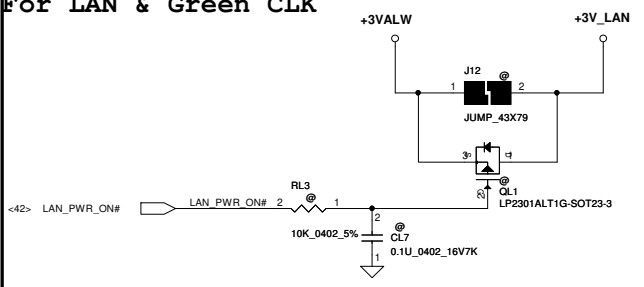
Mini-Express Card for WLAN/WiMAX(Half)



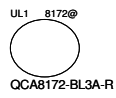
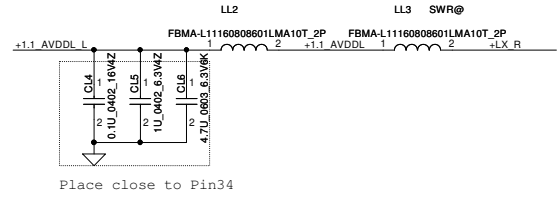
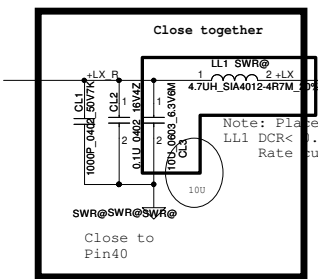
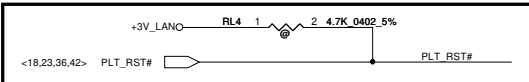
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

| | | | | | |
|---|--------------------|-----------------|--------------------------|-------|-------------------------------|
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| | | | | | VILG1/G2 MB LA9901P Schematic |
| | | | | Date: | Wednesday, March 20, 2013 |
| | | | | Sheet | 36 of 63 |
| | | | | Rev | 1.0 |

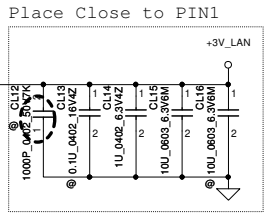
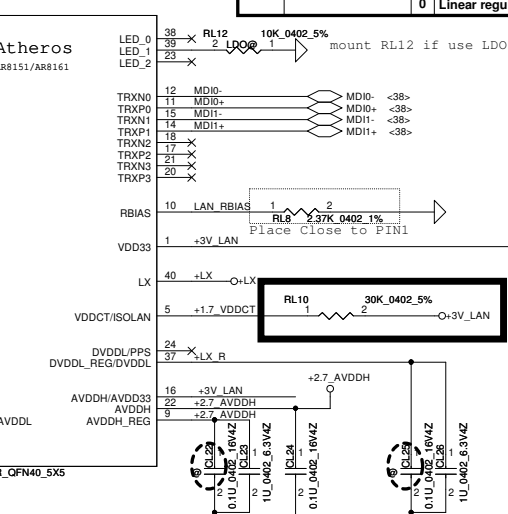
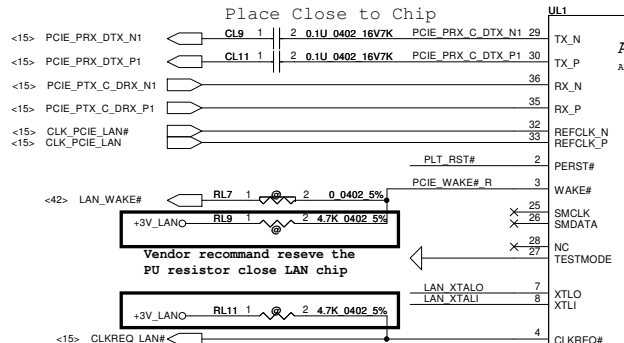
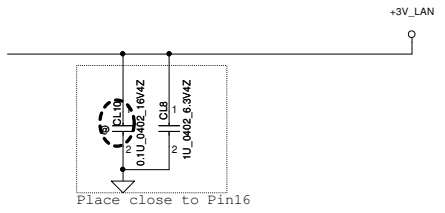
For LAN & Green CLK



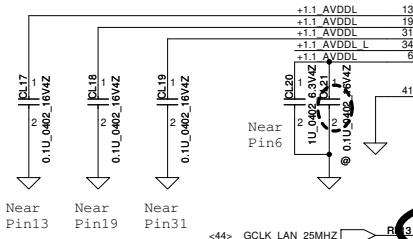
Vendor recommend reseve the
PU resistor close LAN chip



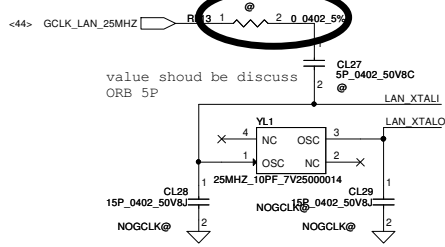
| Pin | Configure signal | Description |
|--------|------------------|-----------------------------------|
| LED[1] | Regulator select | 1 Switch mode regulator(SWR) mode |
| | | 0 Linear regulator (LDO) mode * |



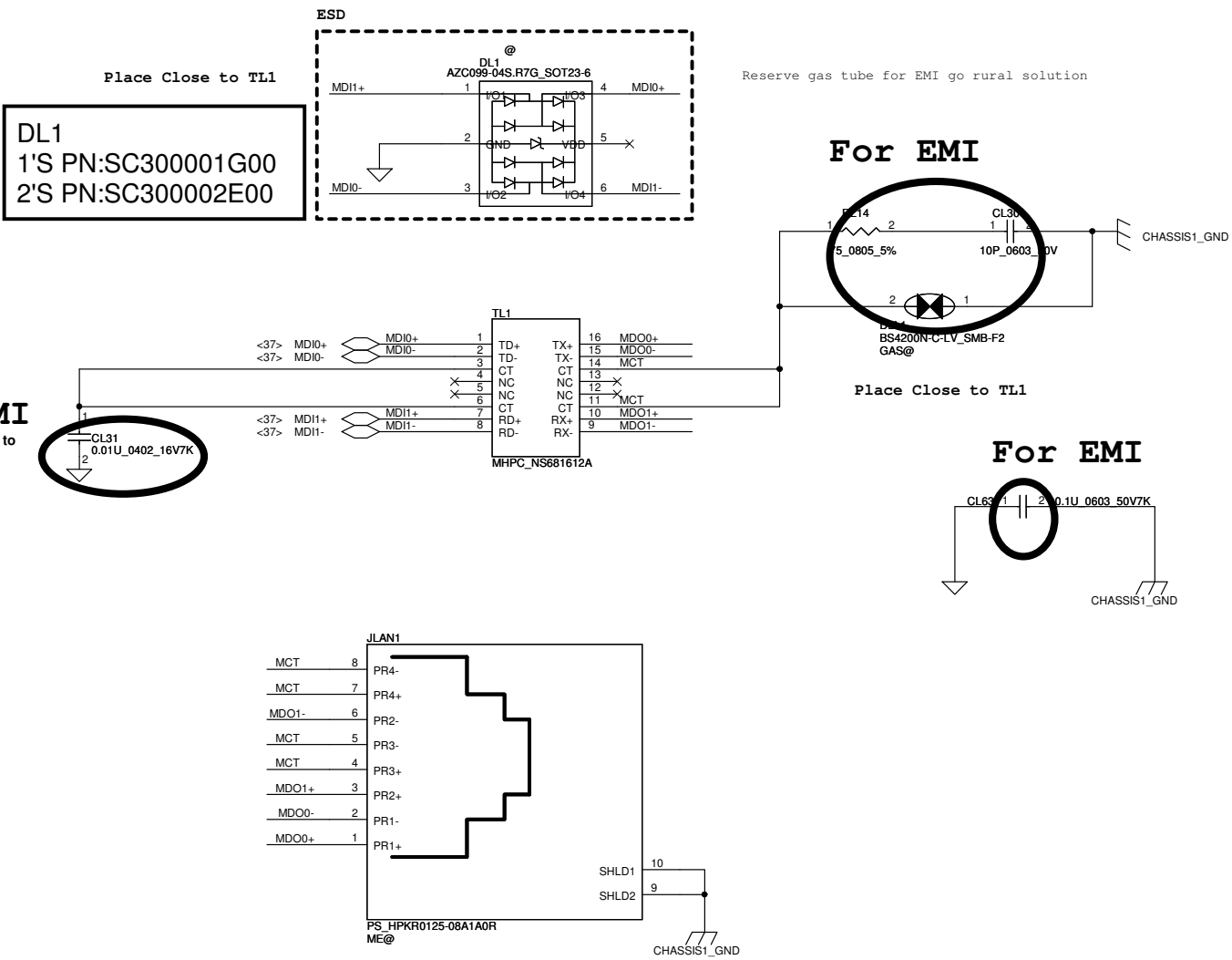
don't @ (could be B C cost done)



For EMI
B Phaes change to GCLK@



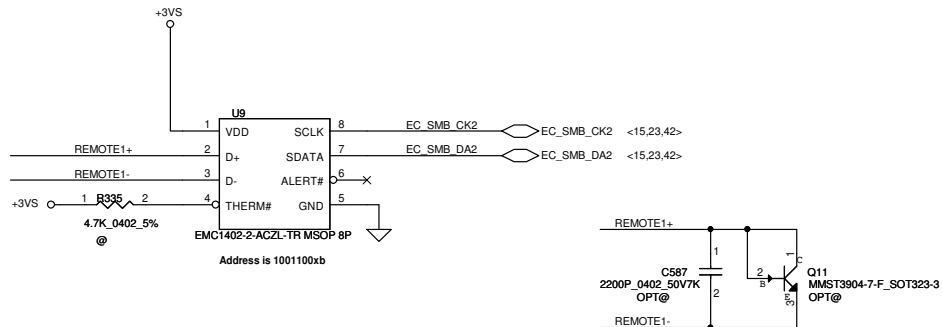
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|---|--------------------|--------------------------|-------------------------------|
| Security Classification | Compal Secret Data | Compal Electronics, Inc. | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |
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| | | Size | Custom |
| | | Document Number | VILG1/G2 MB LA9901P Schematic |
| | | Date | Wednesday, March 20, 2013 |
| | | Sheet | 37 of 63 |



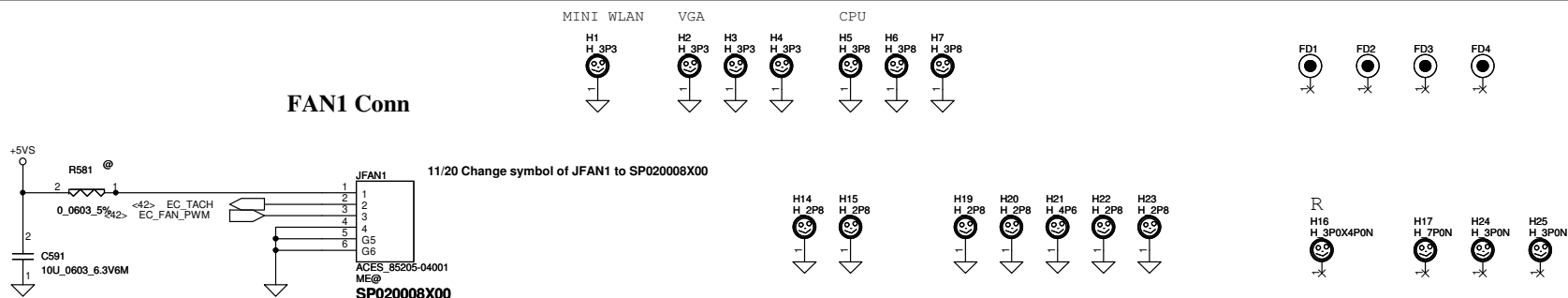
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|---|--|--------------------|--|-----------------|--|---------------------------------|--|-------------------------------|--|---------|--|
| Security Classification | | Compal Secret Data | | | | Compal Electronics, Inc. | | | | | |
| Issued Date | | 2011/06/15 | | Deciphered Date | | 2012/07/11 | | Title | | | |
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| | | | | | | Document Number | | VILG1/G2 MB LA9901P Schematic | | Rev 1.0 | |
| | | | | | | Date: Wednesday, March 20, 2013 | | Sheet 38 of 63 | | | |

2 Channel

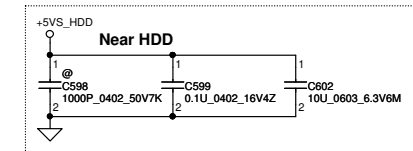
SMSC thermal sensor placed near VRAM



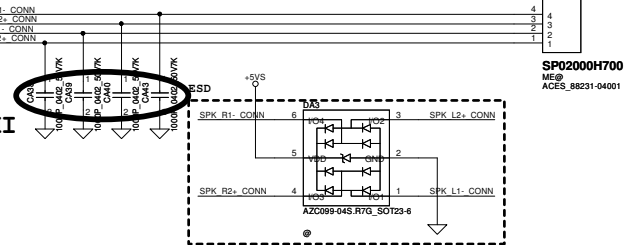
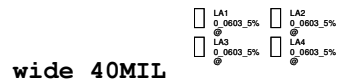
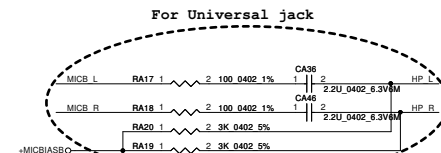
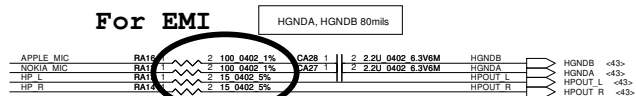
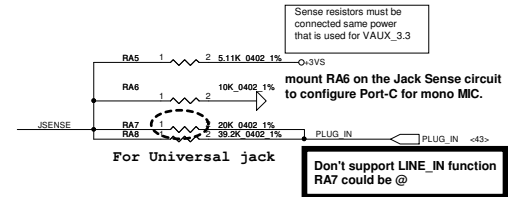
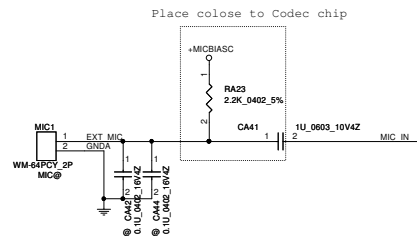
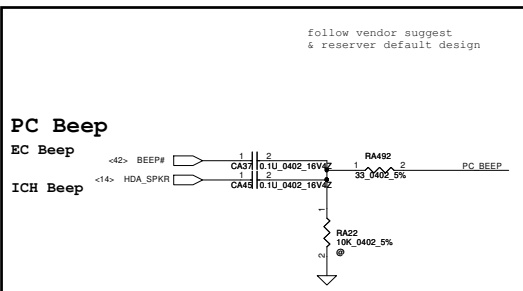
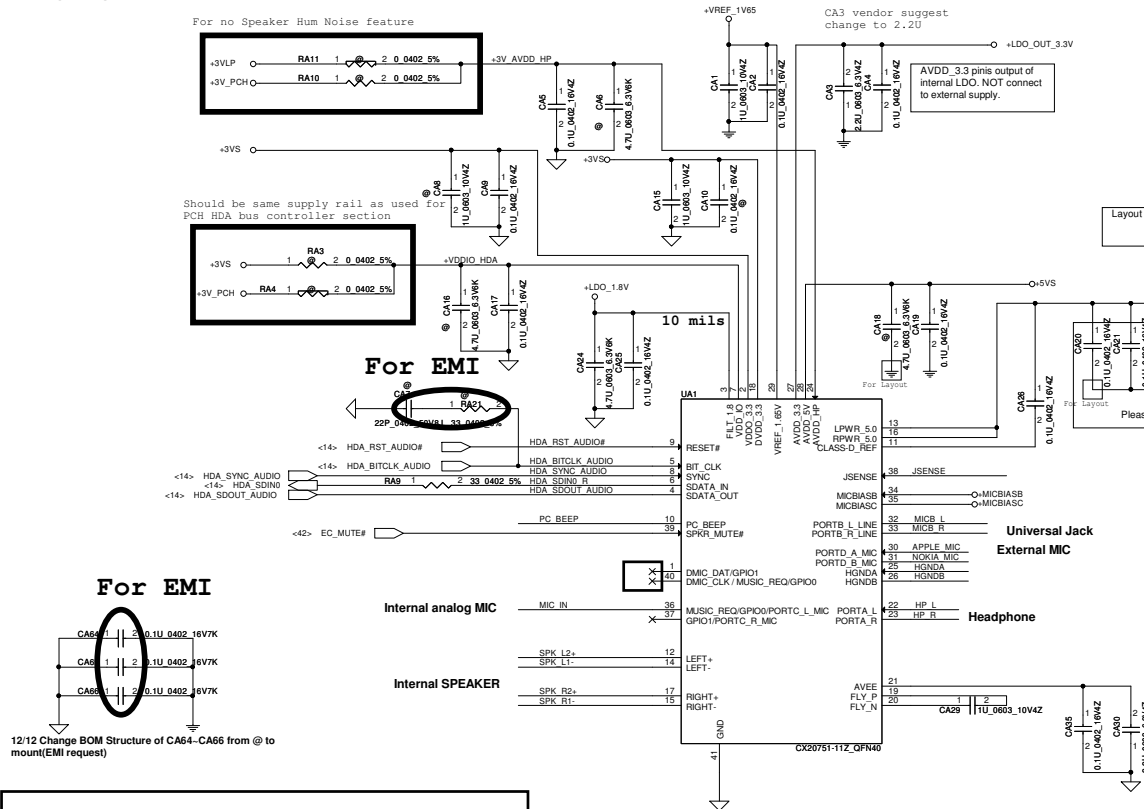
FAN1 Conn



| | | | | | |
|---|------------|--------------------|------------|--------------------------|-------------------------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 | Title | Fintek-Thermal IC/FAN/screw |
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| | | | | Document Number | VILG1/G2 MB LA9901P Schematic |
| | | | | Date | Wednesday, March 20, 2013 |
| | | | | Sheet | 39 of 63 |

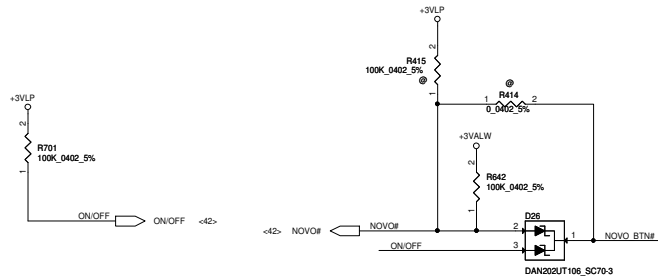


CX20757
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



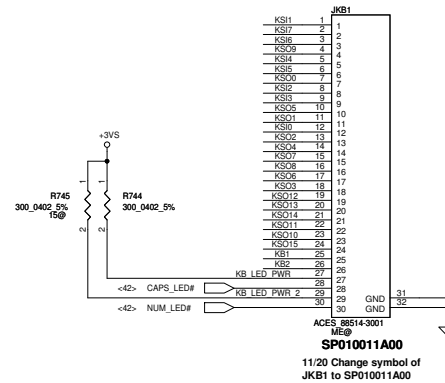
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|---|--------------------|-----------------|------------|---------------------------------|---------------------------|--------|----------|--|--|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | | | | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 | Title | CX20757-112 Codec | | | | |
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| | | | | Current | VILG1/G2 MB LA9901P | Scheme | | | |
| | | | | Date | Wednesday, March 20, 2013 | Sheet | 41 of 63 | | |

PWR Button For Debug

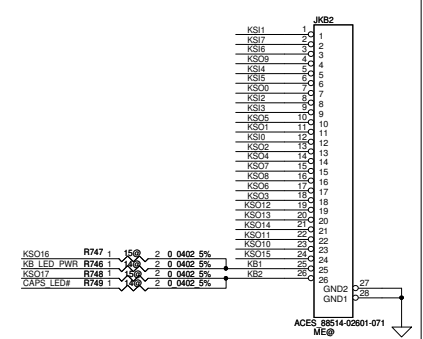


Key Board Conn.

For 15"



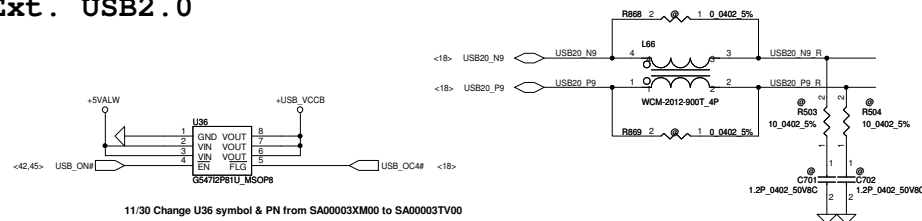
For 14"



IO/B Conn.

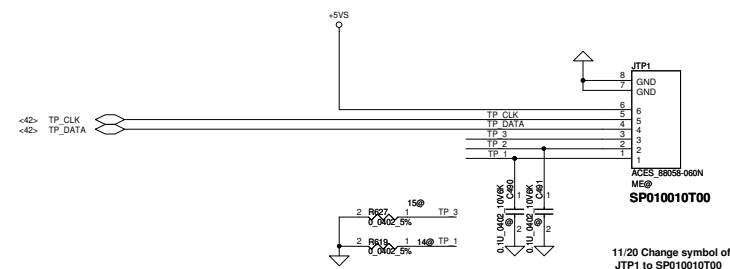
Ext. USB2.0

For EMI

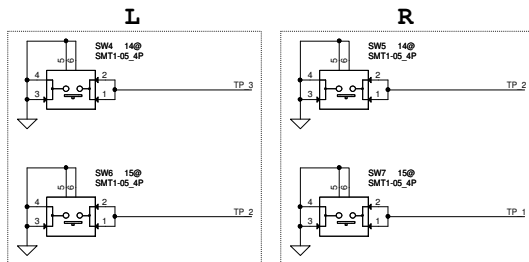


11/30 Change U36 symbol & PN from SA00003XM00 to SA00003TV00

TP Switch & TP Conn.

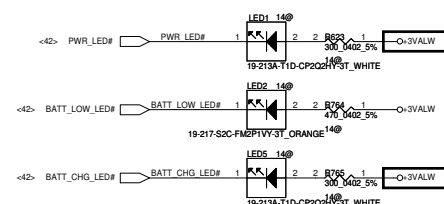


11/20 Change symbol of JTP1 to SP010010T00

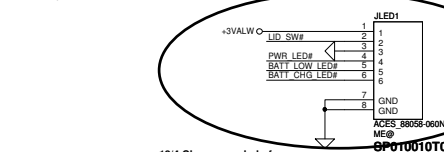


| 15" | 14" |
|-------|-------|
| 1 VCC | 1 VCC |
| 2 CLK | 2 CLK |
| 3 DAT | 3 DAT |
| 4 GND | 4 L |
| 5 L | 5 R |
| 6 R | 6 GND |

LED



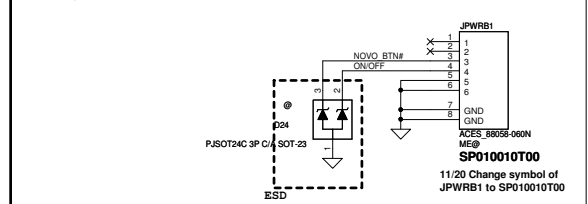
LED/B Conn.



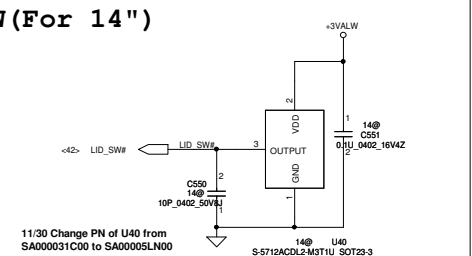
For 15"

12/4 Change symbol of JLED1 to SP010010T00

PWR/B Conn.



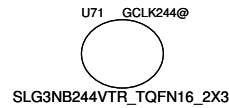
Lid SW(For 14")



11/30 Change PN of U40 from SA000031C00 to SA00005LN00

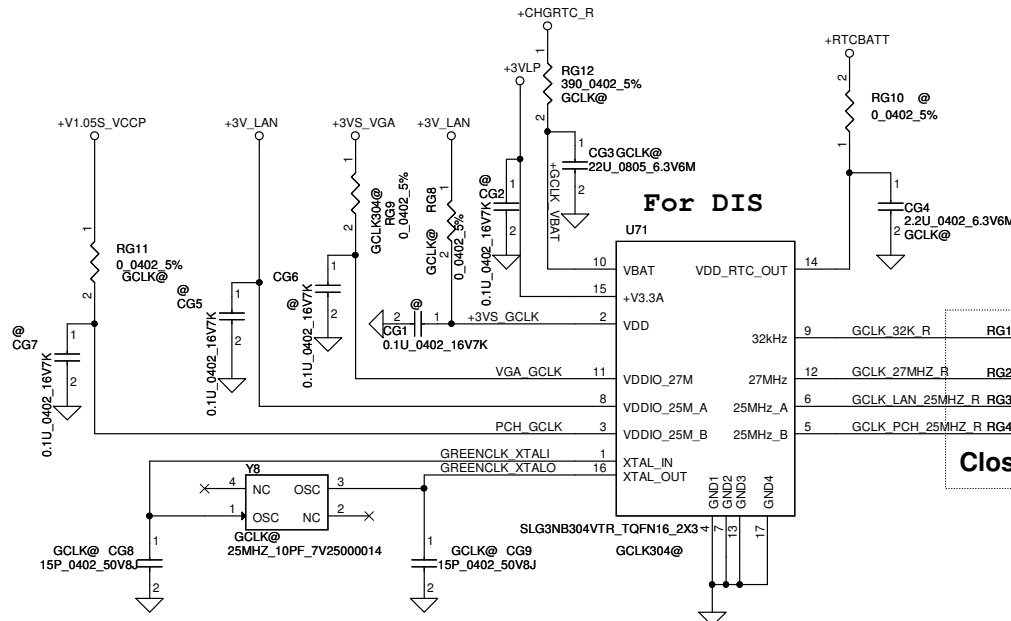
| Security Classification | Compal Secret Data | Document Number | Rev |
|--|---------------------------|-------------------------------|----------|
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| Date: | Wednesday, March 20, 2013 | Sheet | 43 of 63 |

For UMA

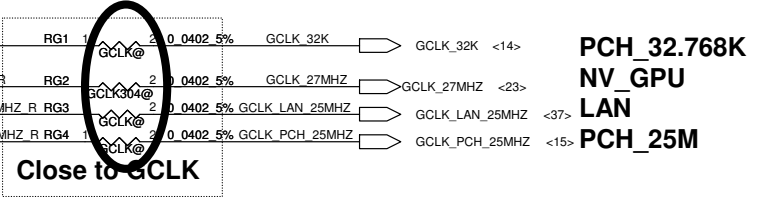


Every power trace need:
W=20mils

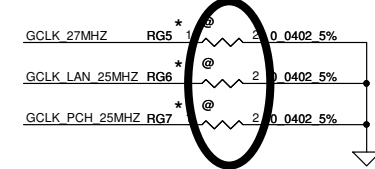
For GreenCLK generate CLK:
Mount: All parts in this page except
Swing Level RES (Marked "**")
NA: PD108,
Y1,R98,C180,C181,
Y2,R169,C196,C197,
Y6,C968,C969



For EMI



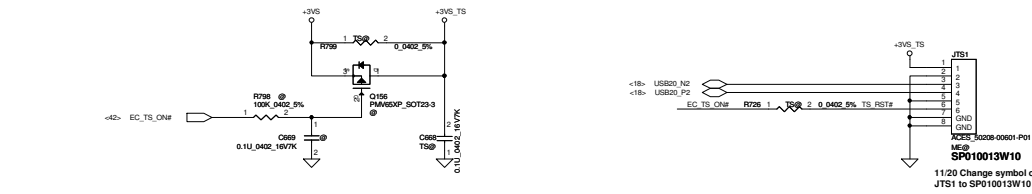
Reserved for Swing Level adjustment
(Close GCLK side)



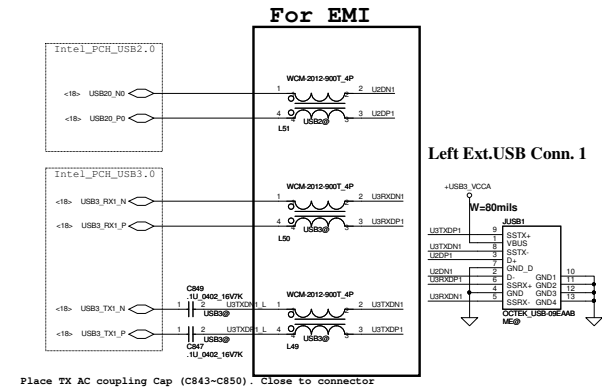
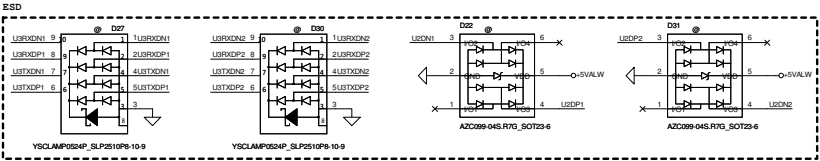
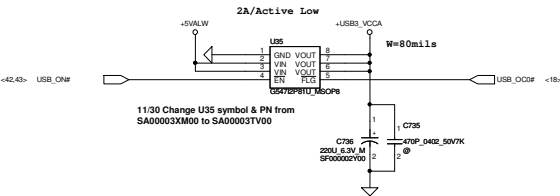
For EMI

| | | | | | |
|---|------------|--------------------|------------|---------------------------------|-----------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 | Title | |
| | | | | USB ext. ports | |
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| | | | | VILG1/G2 MB LA9901P Schematic | |
| | | | | Date: Wednesday, March 20, 2013 | Rev 1.0 |
| | | | | Sheet 44 of 63 | |

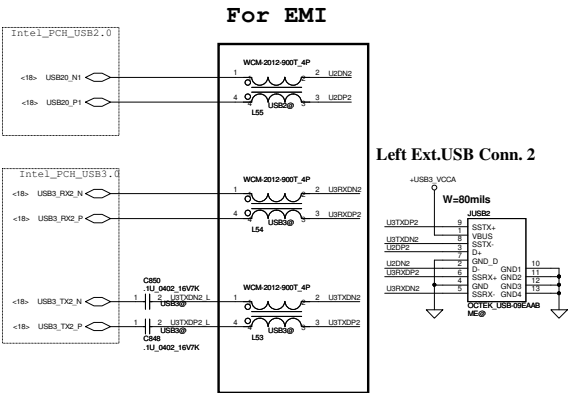
Touch Screen



USB3.0

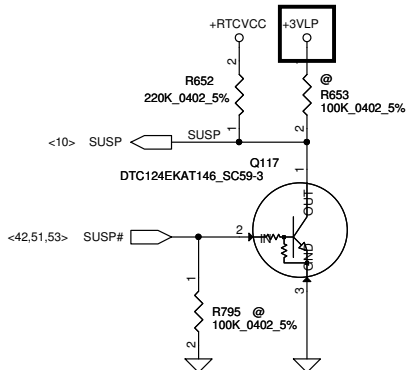
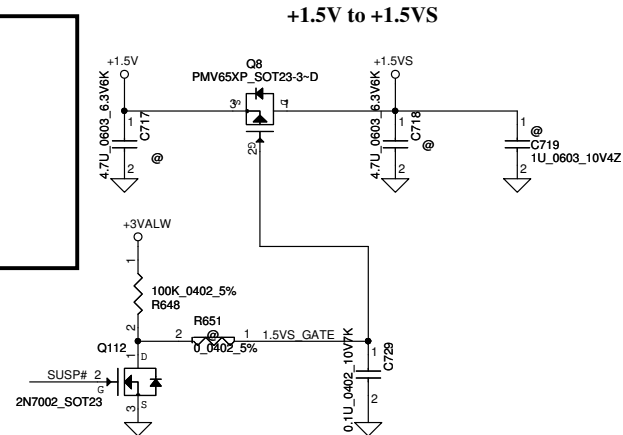
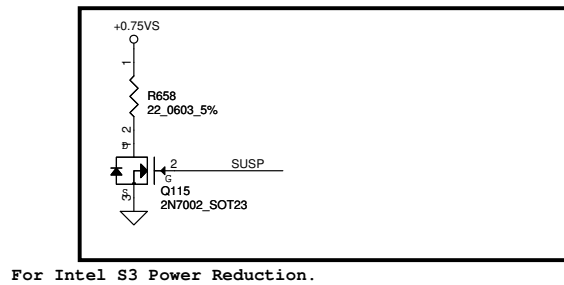
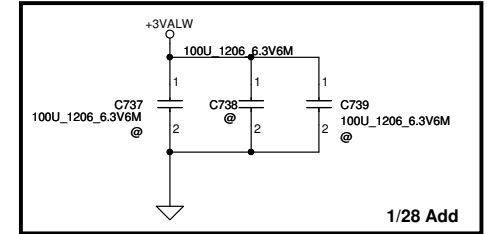
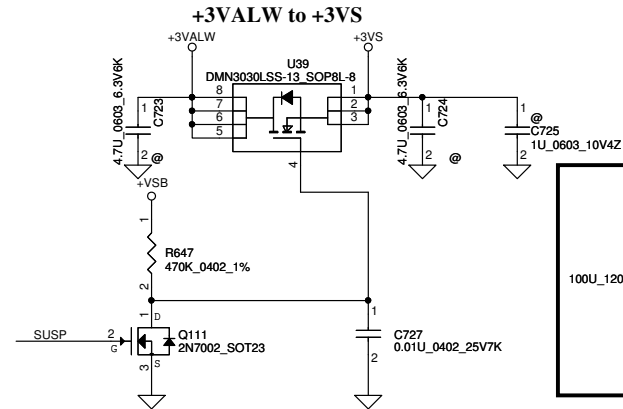
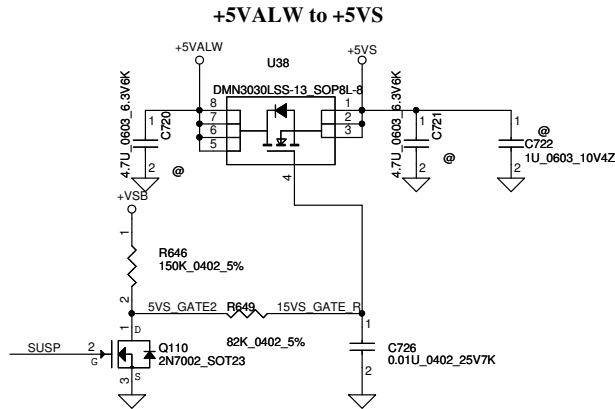


Left Ext.USB Conn. 1



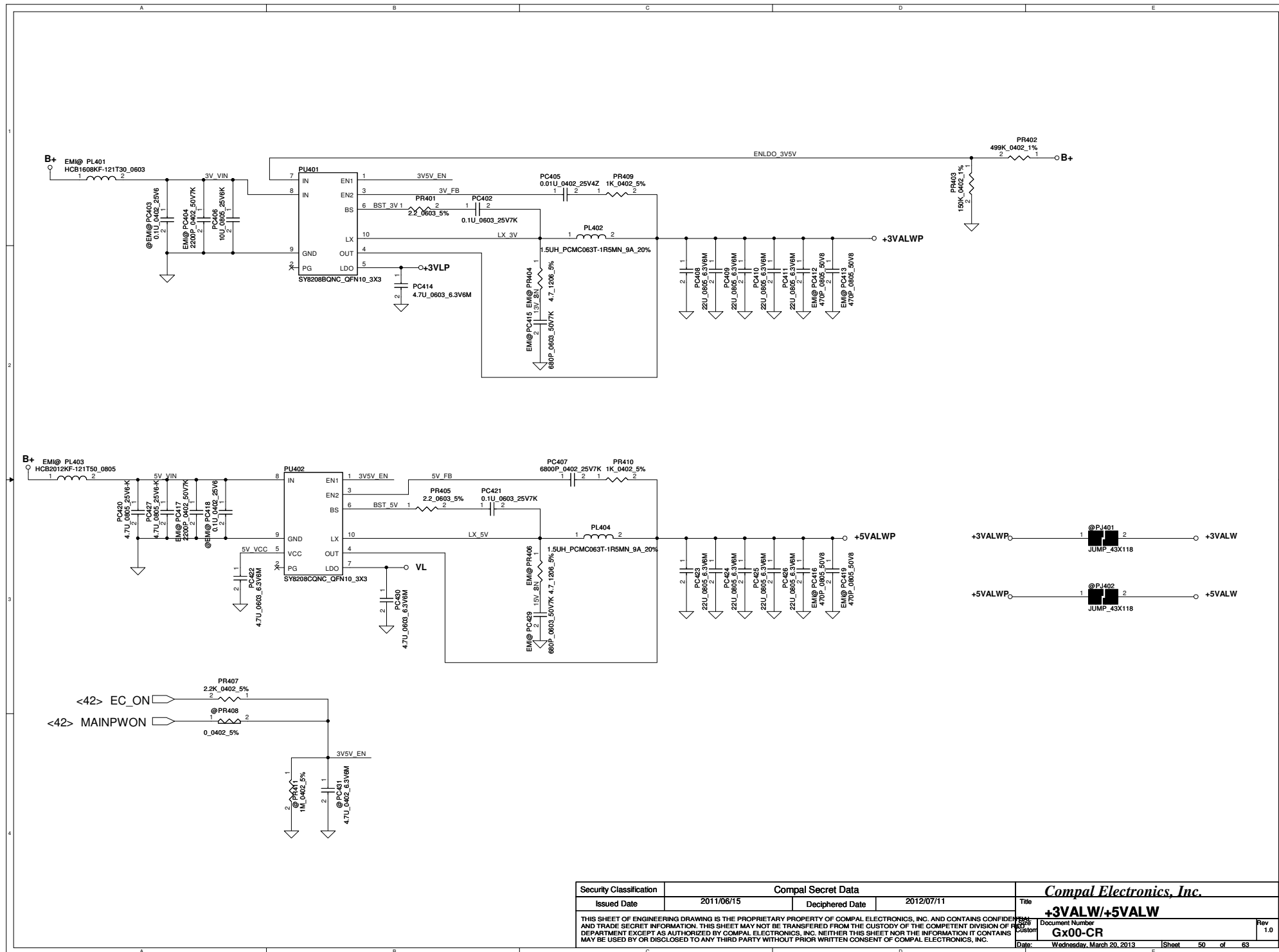
Left Ext.USB Conn. 2

| | | | | |
|--|--------------------|-----------------|--------------------------|--|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 | Title |
| | | | | USB3.0/Left USB Ports |
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| | | | | VILG1/G2 MB LA9901P Schematic |
| | | | | File |
| | | | | Wednesday, March 28, 2012 15:22:45 2/ 55 |

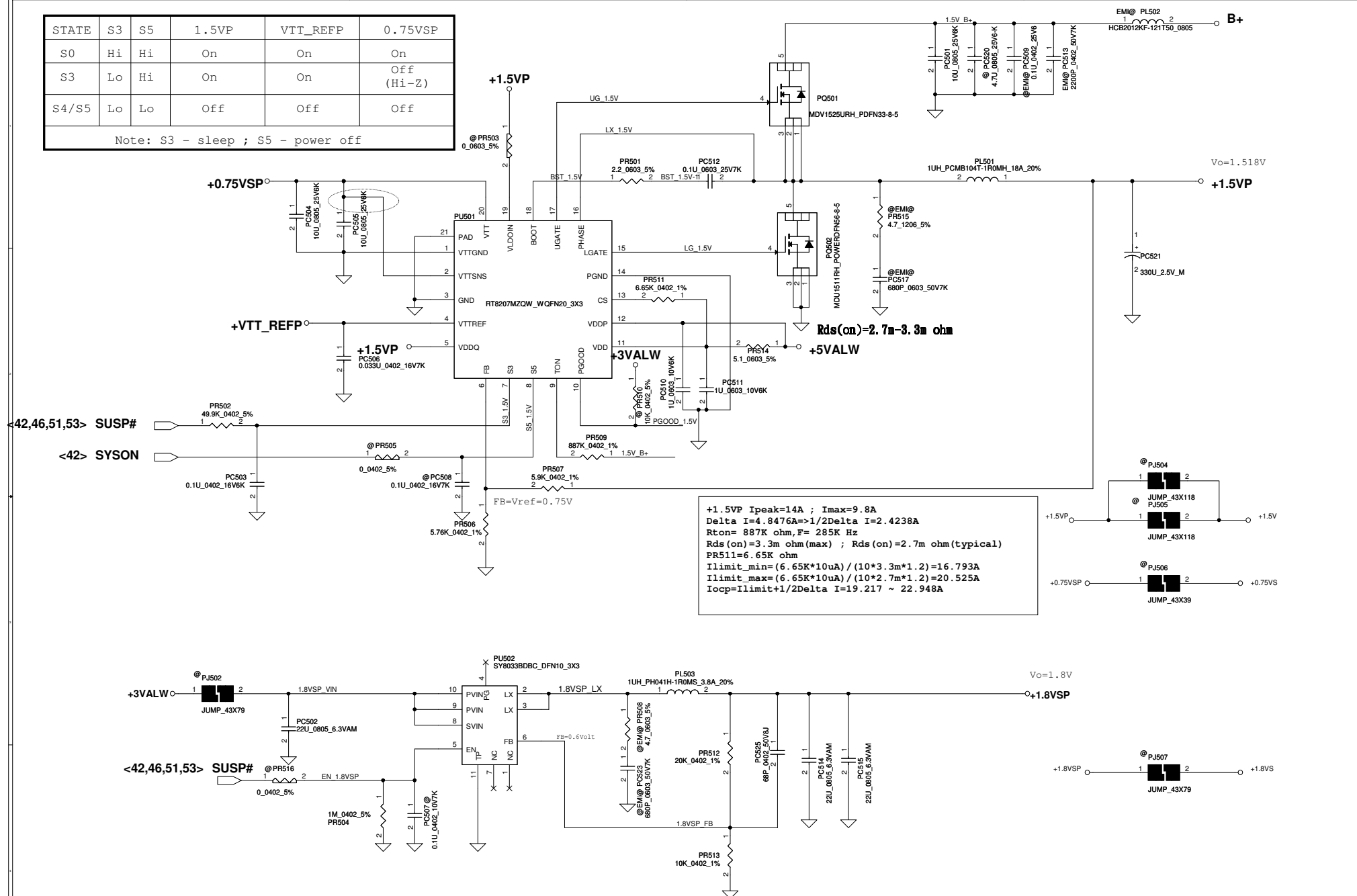


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| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | |
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| | | | | Rev | 1.0 |
| | | | | Date: | Wednesday, March 20, 2013 |
| | | | | Sheet | 46 of 63 |

| | | | | | | |
|---|--------------------|-----------------|------------|--------------------------|----------------------|-------|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 | Title | PWR-BATTERY CONN/OTP | |
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| | | | | Customer | 1.0 | |
| Date: Wednesday, March 20, 2013 | | | | Sheet | 48 | of 63 |



| STATE | S3 | S5 | 1.5VP | VTT_REFP | 0.75VSP |
|-----------------------------------|----|----|-------|----------|---------------|
| S0 | Hi | Hi | On | On | On |
| S3 | Lo | Hi | On | On | Off (Hi-Z) |
| S4/S5 | Lo | Lo | Off | Off | Off |
| Note: S3 - sleep ; S5 - power off | | | | | |



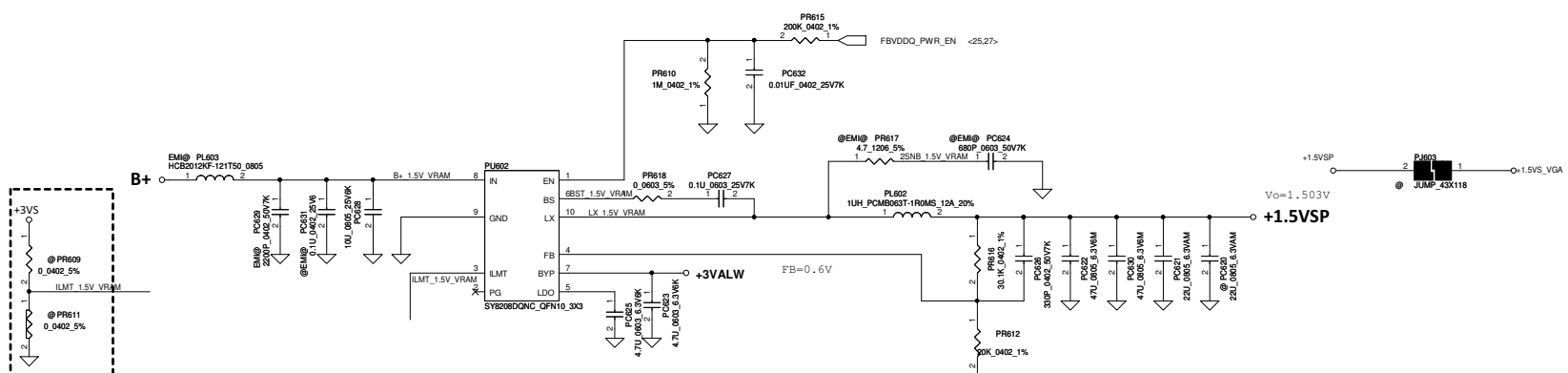
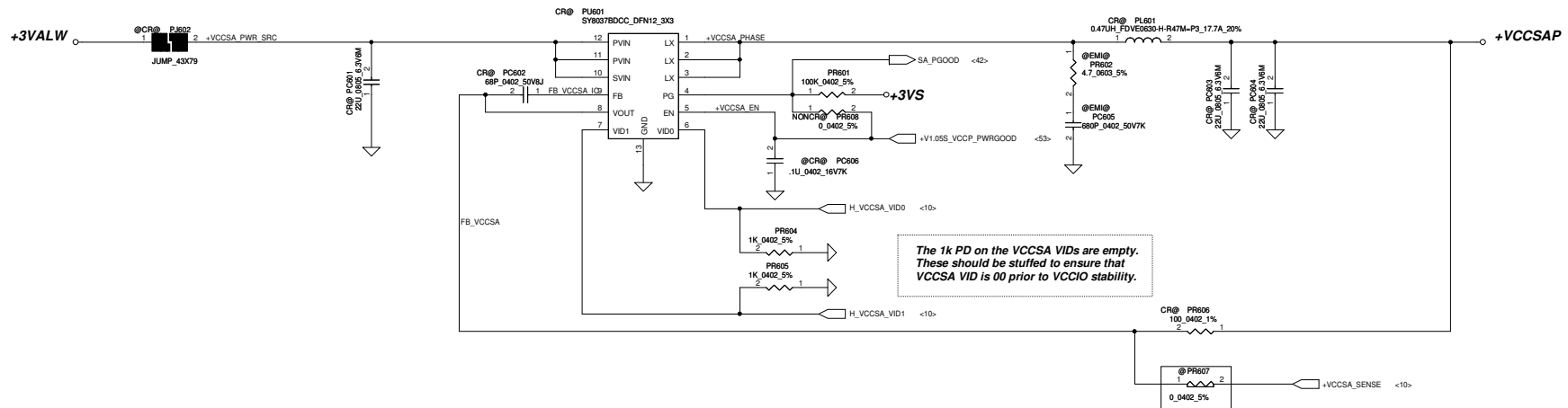
| VID [0] | VID[1] | VCCSA Vout |
|---------|--------|------------|
| 0 | 0 | 0.9V |
| 0 | 1 | 0.8V |
| 1 | 0 | 0.725V |
| 1 | 1 | 0.675V |

output voltage adjustable network

+V1.05S_VCCP $\xrightarrow{0.001, 1206, 1\%}$ +VCCSA

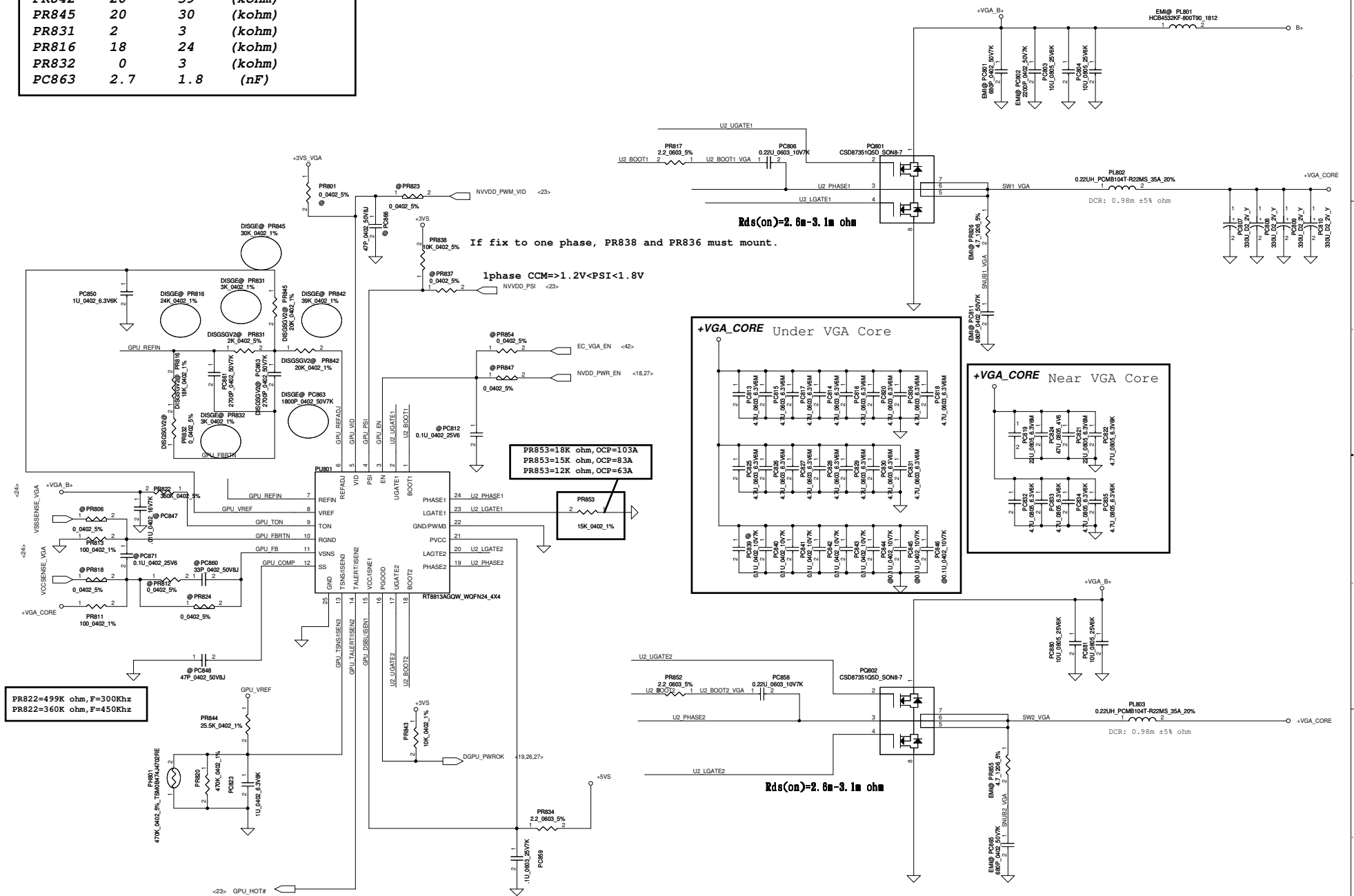
+VCCSAP $\xrightarrow{0.001, 1206, 1\%}$ +VCCSA

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A
OVP 1.06V

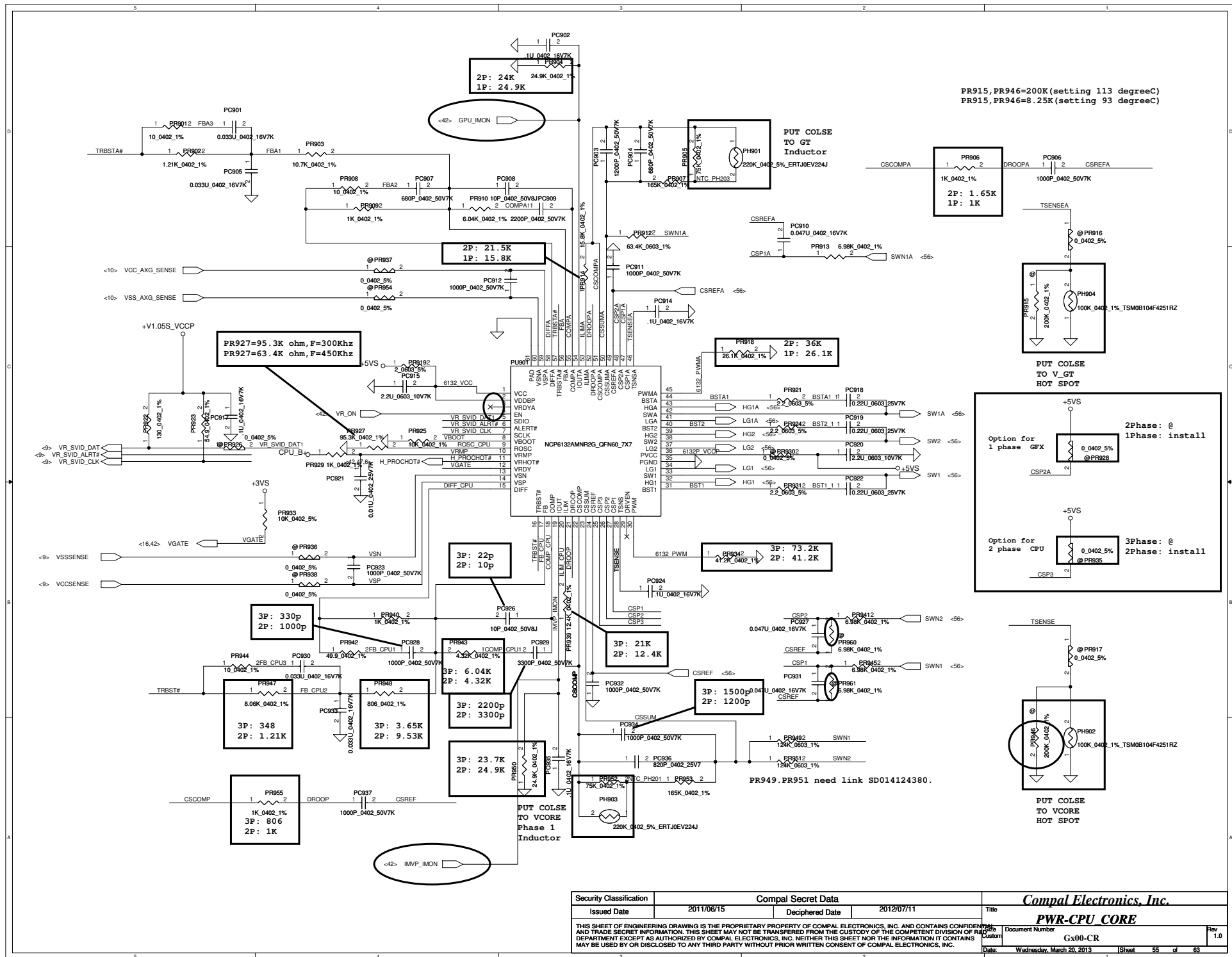


| | | |
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| 2012/07/11 | | Title |
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| | | Gx00-CR |
| | | Size |
| | | 1.0 |
| | | Page |
| | | 1 of 63 |
| | | Revision |
| | | Wednesday, March 20, 2013 |

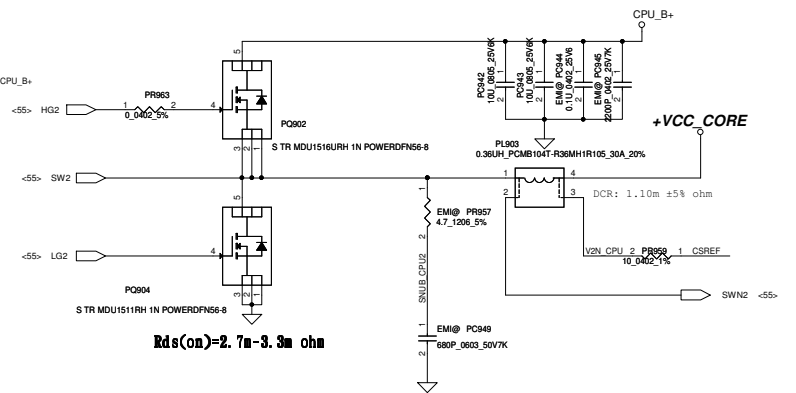
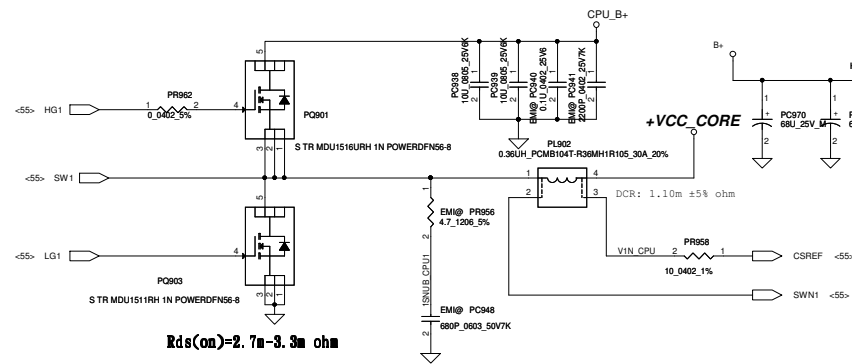
| | GSV2 (25W) | GE (19W) | |
|-------|------------|----------|--------|
| PR842 | 20 | 39 | (kohm) |
| PR845 | 20 | 30 | (kohm) |
| PR831 | 2 | 3 | (kohm) |
| PR816 | 18 | 24 | (kohm) |
| PR832 | 0 | 3 | (kohm) |
| PC863 | 2.7 | 1.8 | (nF) |



| | | | | | |
|---|---------------------------|--------------------|------------|----------|-----|
| Security Classification | | Compal Secret Data | | Title | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 | VGA CORE | |
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| Size | Document Number | Gx00-CR | | Rev | 1.0 |
| Date | Wednesday, March 20, 2013 | Sheet | 54 | of | 63 |

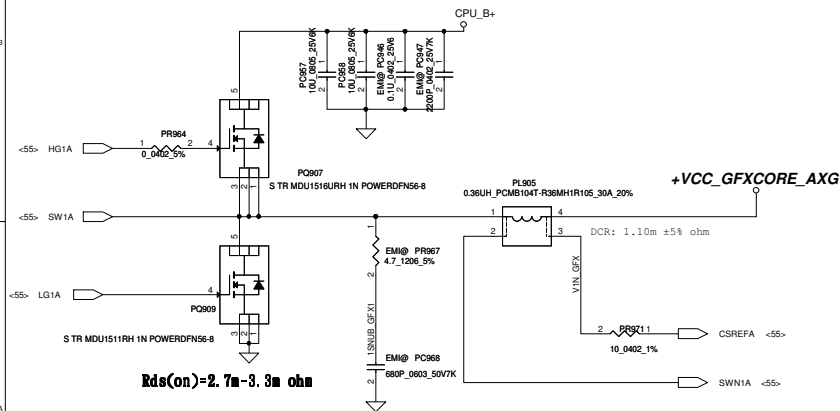


| | | | | |
|---|--------------------|-----------------|--|---|
| Security Classification | Compal Secret Data | | <i>Compal Electronics, Inc.</i> PWR-CPU CORE | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 | Title PWR-CPU CORE Document Number GX00-CR |
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| | | | Date: | Wednesday, March 20, 2013 |
| | | | Sheet | 55 of 63 |



QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP-110A

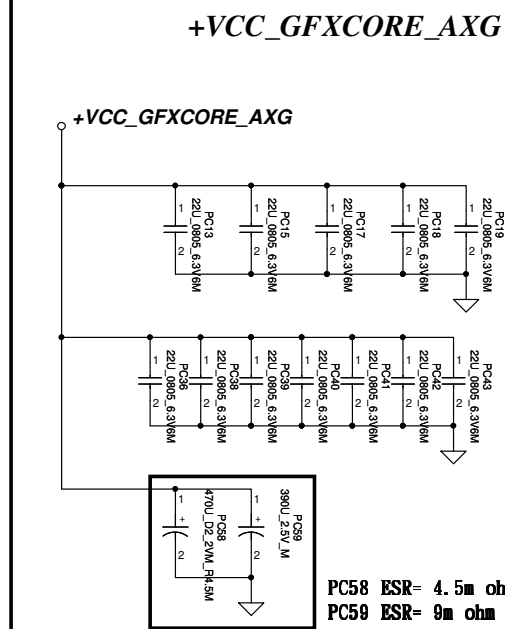
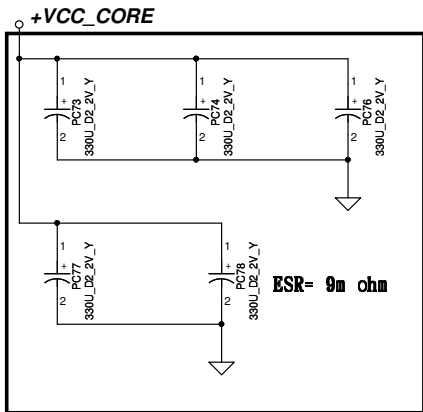
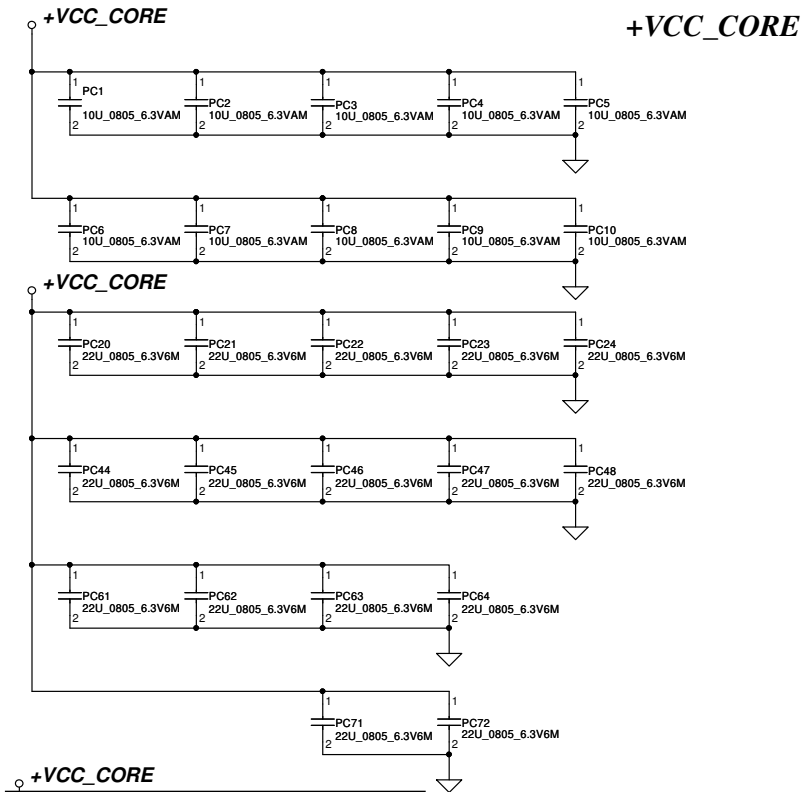
DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP-65A



QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP-55A

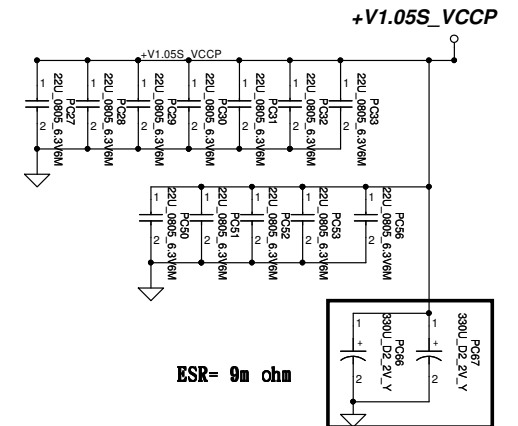
DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP-40A

| | | | | | | | | |
|--|--------------------|-----------------|------------|---------------------------------|-----------------|-----|-------|----------|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | | | | |
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| | | | | Size | Document Number | Rev | | |
| | | | | | Gx00-CR | 1.0 | | |
| | | | | Date: Wednesday, March 20, 2013 | | | Sheet | 56 of 63 |
| | | | | | | | | |



Below is 458544_CRV_PDDG_0.5 Table 5-8.

| | |
|---------------|--|
| Socket Bottom | 5 x 22 μ F (0805) 5 x (0805) no-stuff sites |
| Socket Top | 7 x 22 μ F (0805) 2 x (0805) no-stuff sites |



| | | | | |
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| Size | Document Number | Rev | 1.0 | |
| Date | Wednesday, March 20, 2013 | Sheet | 57 | of 63 |

Version change list (P.I.R. List)

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for PWR

| Item | Reason for change | PG# | Modify List | Date | Phase |
|------|--|-----|---|------------|-------|
| 1 | Design Change of IC Package. | 50 | Change PU401 to SA000061M00(S IC SY8208BQNC QFN 10P PWM) | 2012/11/22 | DVT |
| 2 | Design Change of IC Package. | 50 | Change PU402 to SA000061N00(S IC SY8208CQNC QFN 10P PWM) | 2012/11/22 | DVT |
| 3 | Design Change of IC Package. | 52 | Change PU602 to SA000061Q00(S IC SY8208DQNC QFN 10P PWM) | 2012/11/22 | DVT |
| 4 | Add ADP_ID Circuit. | 47 | Add PQ102 to SB00000E010(S TR 2N7002KDW 2N SOT-363-6 PANJIT) Add PR111.PR112 to SD028100380(S RES 1/16W 100K +-5% 0402) | 2012/12/03 | DVT |
| 5 | Factory lack of material. | 52 | Change PC521 to SF000003H00(S_A-P_CAP 330U 2.5V M 6.3X4.2 LESR16M SL) | 2012/12/06 | DVT |
| 6 | Factory lack of material. | 56 | Change PL902.PL903.PL905 to SH00000N900(S COIL .36U PCMB104T-R36MH1R105 30A GLUE) | 2012/12/06 | DVT |
| 7 | EMI request adjust +3VALWP/+5VALWP snubber function. | 50 | Change @PR404.@PC415.@PR406.@PC429 to PR404.PC415.PR406.PC429. | 2012/12/06 | DVT |
| 8 | EMI request adjust +3VALWP/+5VALWP boost resistor. | 50 | Change PR401.PR405 to SD013220B80(S RES 1/10W 2.2 +-5% 0603). | 2012/12/06 | DVT |
| 9 | EMI request add bypass capacitor. | 50 | Add PC412.PC413.PC416.PC419 to SE001471J80(S CER CAP 470P 50V J NPO 0805 H0.6) | 2012/12/06 | DVT |
| 10 | EMI request adjust CPU/GFX CORE snubber function. | 56 | Change @PR956.@PC948.@PR957.@PC949.@PR967.@PC968 to PR956.PC948.PR957.PC949.PR967.PC968. | 2012/12/06 | DVT |
| 11 | EMI request adjust bypass capacitor. | 56 | Change @PC940 to PC940. | 2012/12/06 | DVT |
| 12 | EMI request add bypass capacitor. | 56 | Add PC944.PC946 to SE00000G880(S CER CAP 0.1U 25V K X5R 0402) Add PC945.PC947 to SE075222K80(S CER CAP 2200P 25V K X7R 0402) | 2012/12/06 | DVT |
| 13 | Design Change of input capacitor. | 50 | Change PC420 to SE000000F80(S CER CAP 4.7U 25V K X6S 0805 H1.25) Add PC427 to SE000000F80(S CER CAP 4.7U 25V K X6S 0805 H1.25) | 2012/12/07 | DVT |
| 14 | Design Change of IC Application. | 50 | Add @PR409.@PR410 to SD028100180(S RES 1/16W 1K +-5% 0402) Add @PC405 to SE075472K80(S CER CAP 4700P 25V K X7R 0402) Add @PC407 to SE075472K80(S CER CAP 0.047U 25V K X7R 0402) Add PR411 to SD028000080(S RES 1/16W 0 +-5% 0402) | 2012/12/10 | DVT |
| 15 | Design Change of IC Application. | 55 | Change PC936 to SE000008980(S CER CAP 820P 25V K X7R 0402) Change PC929 to SE074332K80(S CER CAP 3300P 50V K X7R 0402) Change PC926 to SE071100J80(S CER CAP 10P 50V J NPO 0402) Change PC928 to SE074102K80(S CER CAP 1000P 50V K X7R 0402) Change PR943 to SD000000J280(S RES 1/16W 4.32K +-1% 0402) Change PR949.PR951 to SD014124380(S RES 1/10W 124K +-1% 0603 YAGEO) | 2012/12/17 | DVT |
| 16 | Design Change of CPU/GFX CORE Choke. | 56 | Change PL902.PL903.PL905 to SH00000NM00(S COIL 0.22UH +-20% PCMB104T-R22MS 35A) | 2012/12/21 | DVT |
| 17 | Design Change of VGA CORE(Standby mode Circuit). | 54 | Delete PC864.PQ810.PR802.PR803.PR805 | 2012/12/21 | DVT |
| 18 | Reduction Part Count. | 47 | Delete PR110. | 2013/01/18 | PVT |
| 19 | Reduction Part Count. | 52 | Delete PR603. | 2013/01/18 | PVT |
| 20 | Reduction Part Count. | 54 | Delete PR814.PC849.PR825.PR835.PR850.PD802.PD801. | 2013/01/18 | PVT |

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| | | | | Custom | C38-G series Chief River Schematic |
| | | | | Date: | Wednesday, March 20, 2013 |
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Version change list (P.I.R. List)

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for PWR

| Item | Reason for change | PG# | Modify List | Date | Phase |
|------|---|-----|---|------------|-------|
| 21 | Reduction Part Count. | 55 | Delete PC916. | 2013/01/18 | PVT |
| 22 | Design Change of IC Application. | 50 | Change @PC405.@PR490.@PC407.@PR410 to PC405.PR490.PC407.PR410. Change PR411 to SD028000080(S RES 1/16W 0 +-5% 0402) | 2013/01/18 | PVT |
| 23 | Reduction Part Count. | 51 | Change PR505.PR516 to SD028000080(S RES 1/16W 0 +-5% 0402) Change PR503 to SD013000080(S RES 1/10W 0 +-5% 0603) | 2013/01/18 | PVT |
| 24 | Design Change of Thermal Application. | 51 | Change PC521 to SGA20331E10(S POLY C 330U 2V Y D2 LESR9M EEFSX H1.9) | 2013/01/18 | PVT |
| 25 | Reduction Part Count. | 52 | Change PR611 to SD028000080(S RES 1/16W 0 +-5% 0402) | 2013/01/18 | PVT |
| 26 | Reduction Part Count. | 53 | Change PR702 to SD028000080(S RES 1/16W 0 +-5% 0402) | 2013/01/18 | PVT |
| 27 | Reduction Part Count. | 54 | Change PR823.PR824 to SD028000080(S RES 1/16W 0 +-5% 0402) | 2013/01/18 | PVT |
| 28 | Reduction Part Count. | 55 | Change PR926.PR916.PR917 to SD028000080(S RES 1/16W 0 +-5% 0402) | 2013/01/18 | PVT |
| 29 | Design Change of CPU/GFX CORE Choke. | 56 | Change PL902.PL903.PL905 to SH00000N900(S COIL .36U PCMB104T-R36MH1R105 30A GLUE) | 2013/01/18 | PVT |
| 30 | Design Change of CPU/GFX CORE Frequnce. | 55 | Change PR927 to SD034953280(S RES 1/16W 95.3K +-1% 0402) | 2013/01/18 | PVT |
| 31 | Factory lack of material. | 50 | Change PC420.PC427 to SE000006R80(S CER CAP 4.7U 25V K X5R 0805 H1.25) | 2013/01/18 | PVT |
| 32 | Reduction Part Count. | 50 | Delete PR411. | 2013/01/21 | PVT |
| 33 | Design Change of Power Circuit Application. | 48 | Change PC208 to SE000003J80(S CER CAP 0.068U 16V K X7R 0402) | 2013/01/23 | PVT |
| 34 | Design Change of Power Circuit Application. | 49 | Add PR328 to SD028100280(S RES 1/16W 0 +-5% 0402) Add PR327 to SD028000080(S RES 1/16W 0 +-5% 0402) Add PQ314 to SB000009Q80(S TR 2N7002KW 1N SOT323-3) | 2013/01/23 | PVT |
| 35 | Design Change of Power Circuit Application. | 50 | Change PC405 to SE072103280(S CER CAP .01U 25V Z Y5V 0402) Change PC407 to SE075682K80(S CER CAP 6800P 25V K X7R 0402) | 2013/03/04 | PVT |

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| | | | | C38-G series Chief River Schematic | |
| Date: Wednesday, March 20, 2013 | | | | Sheet | 59 of 63 |

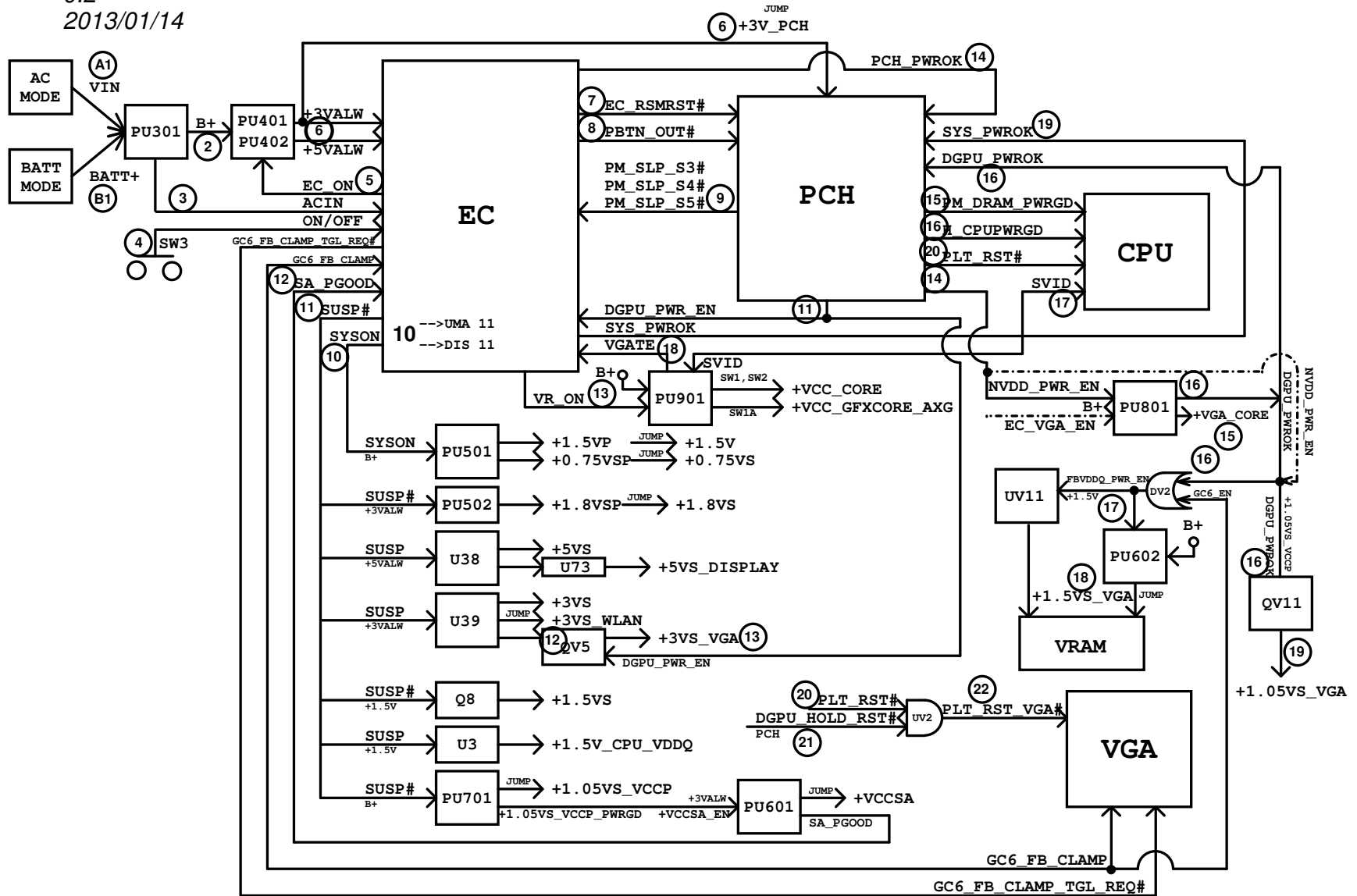
COMPAL CONFIDENTIAL

MODEL NAME: Power Sequence Block Diagram

PCB NAME: LA-9901P

REVISION: 0.2

DATE: 2013/01/14



| | | | | |
|--|--------------------|-----------------|------------|---------------------------------|
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| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 | Power sequence |
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| | | | | Rev 1.0 |
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VILG1/G2 HW PIR List

| Item | Page | MODIFICATION LIST | PURPOSE | EVT TO DVT |
|------|---------|--|---|------------|
| 1 | P. 5~11 | Change footprint of JCPU1 | For Lenovo rule | |
| 2 | P. 14 | Add R406, R407, R408, R409 | Reserve for improvement factory processes | |
| 3 | P. 42 | Add EC_SPI_SO, EC_SPI_SI, EC_SPI_CLK, EC_SPI_CS# to EC | Reserve for improvement factory processes | |
| 4 | P. 42 | Add PCH_PWR_EN to EC Pin.107 | Reserve for improvement factory processes | |
| 5 | P. 42 | Reserve R410 | Reserve Pull-high for GPIO use | |
| 6 | P. 42 | Change EC_FAN_PWM from EC Pin.34 to EC Pin.26 | For common design | |
| 7 | P. 42 | Change NOVO# from EC Pin.26 to EC Pin.34 | For common design | |
| 8 | P. 42 | Change ENBKL from EC Pin.73 to EC Pin.76 | For common design | |
| 9 | P. 42 | Change IMVP_IMON from EC Pin.76 to EC Pin.73 | For common design | |
| 10 | P. 42 | Change DGPU_PWR_EN from EC Pin.107 to EC Pin.123 | For common design | |
| 11 | P. 42 | Change OVERT#_R from EC Pin.117 to EC Pin.17 | For common design | |
| 12 | P. 34 | Add R411, R412, C411, C412 | Reserve for EMI | |
| 13 | P. 20 | Add Q21, R40, C237, Q22,R418, C243,C252,R413 | Reserve for power consumption | |
| 14 | P. 25 | Change RV41 to 1K ohm, CV63 to 1uF | For VGA Sequence | |
| 15 | P. 25 | Add QV4/RV42 | For VGA Sequence | |
| 16 | P. 25 | Change QV3/UV11 | For VGA Sequence | |
| 17 | P. 26 | Change RV241 to 15K ohm | For VGA Sequence | |
| 18 | P. 26 | Add QV6 and RV44. | For VGA Sequence | |
| 19 | P. 26 | Change QV10/QV11 | For VGA Sequence | |
| 20 | P. 43 | Del Q12/R806 | For Change Audio Jack type from Normal close to Normal open | |

VILG1/G2 HW PIR List

| Item | Page | MODIFICATION LIST | PURPOSE | DVT TO PVT |
|------|-------|---|---|------------|
| 1 | P. 36 | Reserve R508 | For leakage current issue of Atheros WLAN | |
| 2 | P. 41 | Change RA22 to reserve | For PC Beep issue(can't heard sound of "di" on BIOS setup menu) | |
| 3 | P. 41 | Reserve RA10/RA11 | For solve Codec speaker Hum noise issue(Zizi) | |
| 4 | P. 42 | Reserve R416 | Reserve +3VLP power rail to EC | |
| 5 | P. 42 | Change EC_RST# power rail to +3V_EC | Using power rail which the same with EC | |
| 6 | P. 42 | Change EC_SMB_CK1 & EC_SMB_DA1 power rail to +3V_EC | Using power rail which the same with EC | |
| 7 | P. 14 | Change U5 from 4MB to 8MB ROM | Follow common design | |

| | | | | |
|---|-------|--|-------------------------|---------------|
| 1 | P. 23 | Change RV5 to shortpad | | PVT TO Pre-MP |
| 2 | P. 42 | Chagne R416 to shortpad | | |
| 3 | P. 52 | Reserve +1.05S_VCCP_PWRGOOD of +V1.05S_VCCP to connect to SA_PGOOD | For Celeron/Pentium CPU | |

Page 3 of 3 for HW PIR

[illegible]

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|--|---------------------------|-----------------|------------|--------------------------------------|----------------|----|
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| | | | | VILG1/G2 MB LA9901P Schematic | 1.0 | |
| Date | Wednesday, March 20, 2013 | | Sheet | 63 | of | 63 |